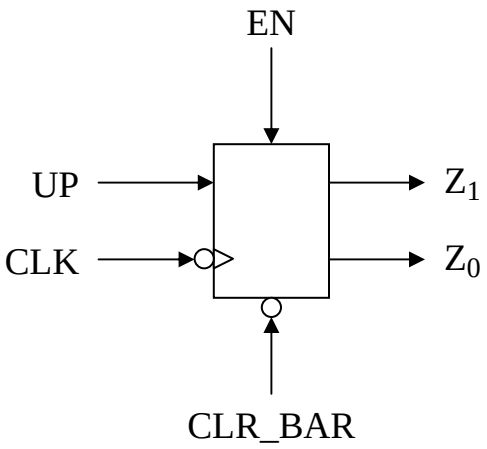
Experiment 9

Synchronous Sequential Design

Design a synchronous sequential Moore machine which implements a 2-bit binary counter with the following characteristics:



- An active-high enable, EN
  - When EN = 1, the counter changes state
  - When EN = 0, the counter maintains its current state
- An active-high control signal, UP
  - When UP = 1, the counter counts up in the sequence 00, 01, 10, 11, 00, …
  - When UP = 0, the counter counts down in the sequence 00, 11, 10, 01, 00, …
- An active-low asynchronous clear, CLR_BAR
  - When CLR_BAR = 0, the count is reset to 00
- A falling-edge triggered clock, CLK

To complete this experiment do the following:

1. Draw a state diagram which represents the Moore machine described above.
2. Fill in the state table below for the Next States and determine Excitation Variables necessary to implement the state machine using JK flip-flops.
3. Minimize the Boolean equations for the Excitation Variables.
4. Draw a detailed circuit diagram for the state machine, showing all pin connections.
5. Implement your circuit in hardware, using TTL parts, and verify its operation.
6. Write a VHDL structural description to implement the circuit, including the following:
   a. Entity declaration.
   b. Structural architecture body using components from the **ece332_gates** package.
   c. A testbench which demonstrates correct operation of the circuit.
7. Simulate your VHDL model and print the resulting waveforms.
8. Compare the results of the two implementations.

	Inputs		Present State		Next State		Excitation Variables				Outputs	
mt	EN	UP	Q_1	Q_0	Q_1^+	Q_0^+	J_1	K_1	J_0	K_0	Z_1	Z_0
0	0	0	0	0							0	0
1	0	0	0	1							0	1
2	0	0	1	0							1	0
3	0	0	1	1							1	1
4	0	1	0	0							0	0
5	0	1	0	1							0	1
6	0	1	1	0							1	0
7	0	1	1	1							1	1
8	1	0	0	0							0	0
9	1	0	0	1							0	1
10	1	0	1	0							1	0
11	1	0	1	1							1	1
12	1	1	0	0							0	0
13	1	1	0	1							0	1
14	1	1	1	0							1	0
15	1	1	1	1							1	1