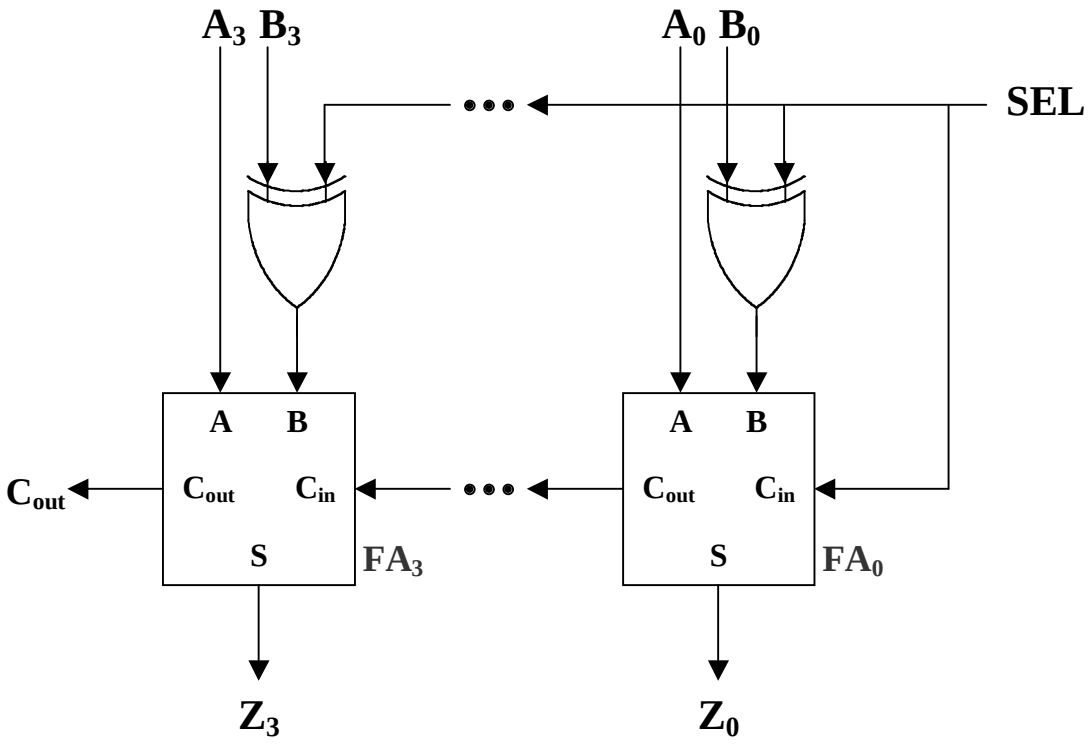
Experiment 8

4-bit Adder-Subtractor



The circuit diagram above implements a 4-bit adder-subtractor:

$$SEL = 0 \Rightarrow Z = A + B$$

$$SEL = 1 \Rightarrow Z = A + \overline{B} + 1 = A - B$$

1. Write a VHDL **package** containing behavioral descriptions of an *XOR* gate and a *Full Adder*.
2. Write a VHDL structural description to implement the circuit, including the following:
   a. Entity declaration
   b. Structural architecture body using **generate** statements for the regular structures

c. A testbench which demonstrates correct operation of the circuit with an example of each of the following cases:

A	**B**	**A + B**	**A - B**
4	2		
2	5		
-3	-4		
-2	6		
6	3		

3. Simulate and print the resulting waveforms for the cases listed above.
4. Design an MSI implementation of the circuit using a 4-bit adder and draw a detailed diagram showing all the pin connections.
5. Implement the circuit in hardware, using the TTL devices from the parts list and verify its operation using the test vectors above.
6. Compare the results of the two approaches with respect to the timing characteristics of the outputs.