Experiment 7

Integrated Circuit Technology Lab

As a digital systems designer, you will need to be aware of the electrical characteristics of various logic families, because a design must be logically *and* electrically correct to ensure proper operation. Even if a design is logically correct, it may fail to operate correctly if the design violates electrical limitations and usage rules of a particular logic family.

In this lab you will do a comparative study of the 74LS00 Quad 2-input AND gate and the 74C00, a CMOS version of the same device.

1. Using the respective datasheets for the two devices, determine the following electrical characteristics and compare the results for the TTL and CMOS families.
   a. Noise Margin
   b. Fan-out
   c. Propagation Delay
2. Use a dual-trace oscilloscope to observe the actual propagation delays for the two devices. Inject a square wave into the selected channel and compare the input signal with the output signal by displaying them simultaneously on the two channels. Record your observations and comment on the difference in behavior between the TTL and CMOS devices, as well as the differences in observed behavior with that determined in part 1c above.
3. Based on your observed results in part 2 above, write VHDL **package** containing behavioral models for both the TTL and CMOS devices. Use a **generic** clause to model the propagation delay.
4. Write a VHDL structural model and associated testbench that will instantiate each device model with the appropriate propagation delay. Simulate your VHDL model to demonstrate that you have correctly modeled the behavior observed in part 2 above.

Hint: For the CMOS gate, output currents are named I_{source} and I_{sink}. Make sure you use the V_{cc} = 5V parameters.