Experiment 2

Given the following function:

$$f(S,E,A,L) = \Sigma m(0,2,3,5,8,9,11,13,15) + d(1,4,10)$$

1. Using a K-map, determine a minimal sum-of-products covering of the function, using "don't cares" as appropriate.
2. Draw a gate level circuit diagram implementing the K-map derived function, using only AND, OR and NOT gates.
3. Write a VHDL structural description to implement your circuit at the gate level, using the pre-defined gate libraries. Be sure to including the following:
a. Entity declaration
b. Structural architecture body
c. Combinational architecture
d. An appropriate testbench
4. Simulate and print the resulting waveforms for all possible inputs.
5. Draw a detailed diagram showing all the pin connections.
6. Implement the circuit in hardware, using the TTL devices from the parts list.
7. Compare the results of the two approaches with respect to the timing characteristics of the outputs.