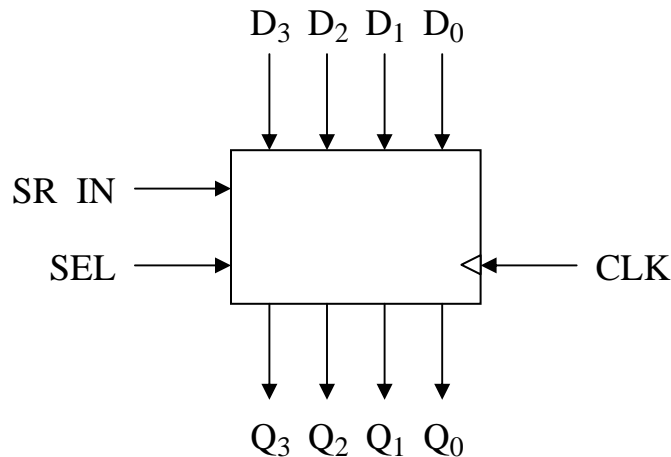


## Experiment 10

### Shift Register

Design a *4-bit parallel input / parallel output shift register* with the following characteristics:



- An mode control signal, SEL
  - When SEL = 0, the register loads  $D_i$
  - When SEL = 1, the register shifts right (and  $Q_3$  receives SR\_IN)
- A rising-edge triggered clock, CLK

To complete this experiment do the following:

1. Draw the circuit diagram for the *shift register* described above, using D flip-flops and 2 to 1 multiplexers.
2. Implement your circuit in hardware, using TTL parts, and verify its operation.
3. Write a VHDL behavioral description which implements this *shift register*, including the following:
  - a. Entity declaration
  - b. Dataflow architecture body
  - c. An appropriate testbench
4. Simulate your VHDL model and print the resulting waveforms.
5. Compare the results of two implementations.