HMK #9

(2) P_{op_delay}

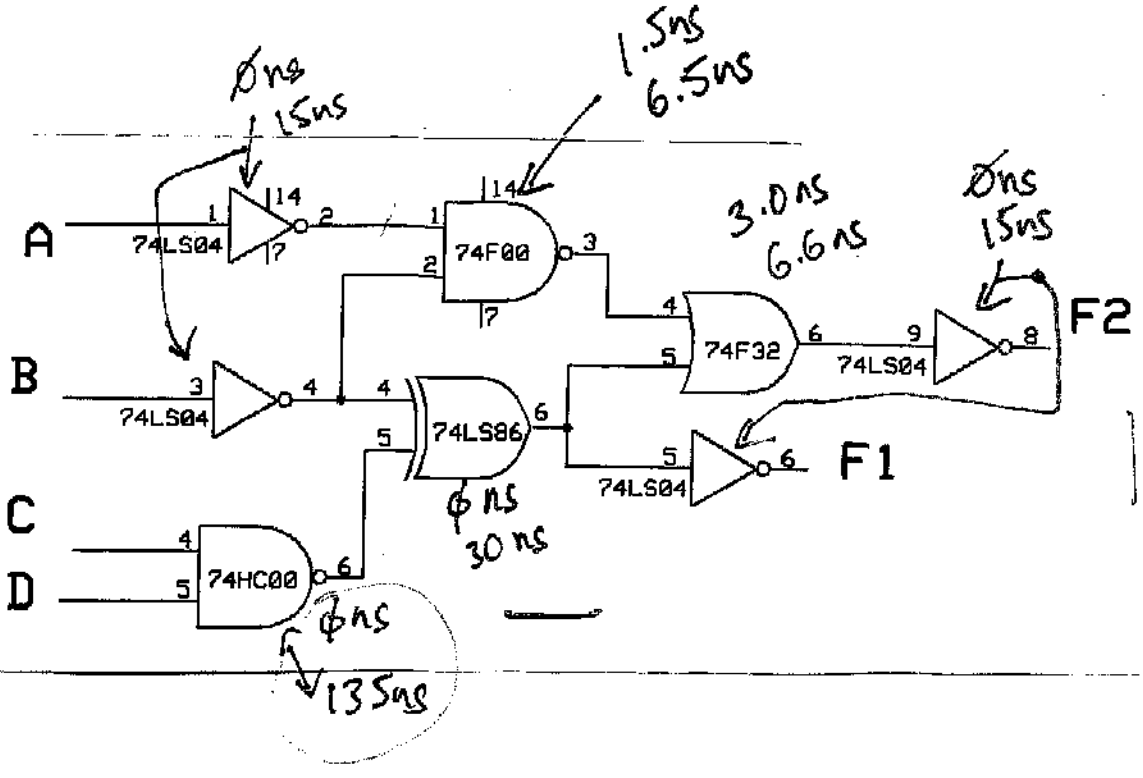
ON Semiconductor 74LS04
min = 0 ns
max = 15 ns

ON Semiconductor 74LS08
min = 0 ns
max = 30 ns

when Vcc = 2V
Philips 74HC00
min = 0 ns
max = 135 ns ? X

Philips 74F32
min = 3.0 ns
max = 6.6 ns

Philips 74F00
min = 1.5 ns
max = 6.5 ns



F1

SBC

Input B $0ns + 0ns + 0ns = 0ns$

Input C+D $0ns + 0ns + 0ns = 0ns$

SWC

Input B $15ns + 30ns + 15ns = 60ns$

Input C+D $135ns + 30ns + 15ns = 180ns$ X

$\therefore$ Maximum Propagation Delay = 180ns Y

Minimum Propagation Delay = 0ns

F2

SBC

Input A $0ns + 1.5ns + 3.0ns + 0ns = 4.5ns$

Input B $0ns + 0ns + 3.0ns + 0ns = 3.0ns$

Input C+D $0ns + 0ns + 3.0ns + 0ns = 3.0ns$

SWC

Input A $15ns + 6.5ns + 6.6ns + 15ns = 43.1ns$

Input B $15ns + 30ns + 6.6ns + 15ns = 66.6ns$

Input C+D $135ns + 30ns + 6.6ns + 15ns = 186.6ns$ X

$\therefore$ Maximum Propagation Delay = 186.6ns

Minimum Propagation Delay = 3.0ns

3a) $X = \bar{A}D + B$ ✓

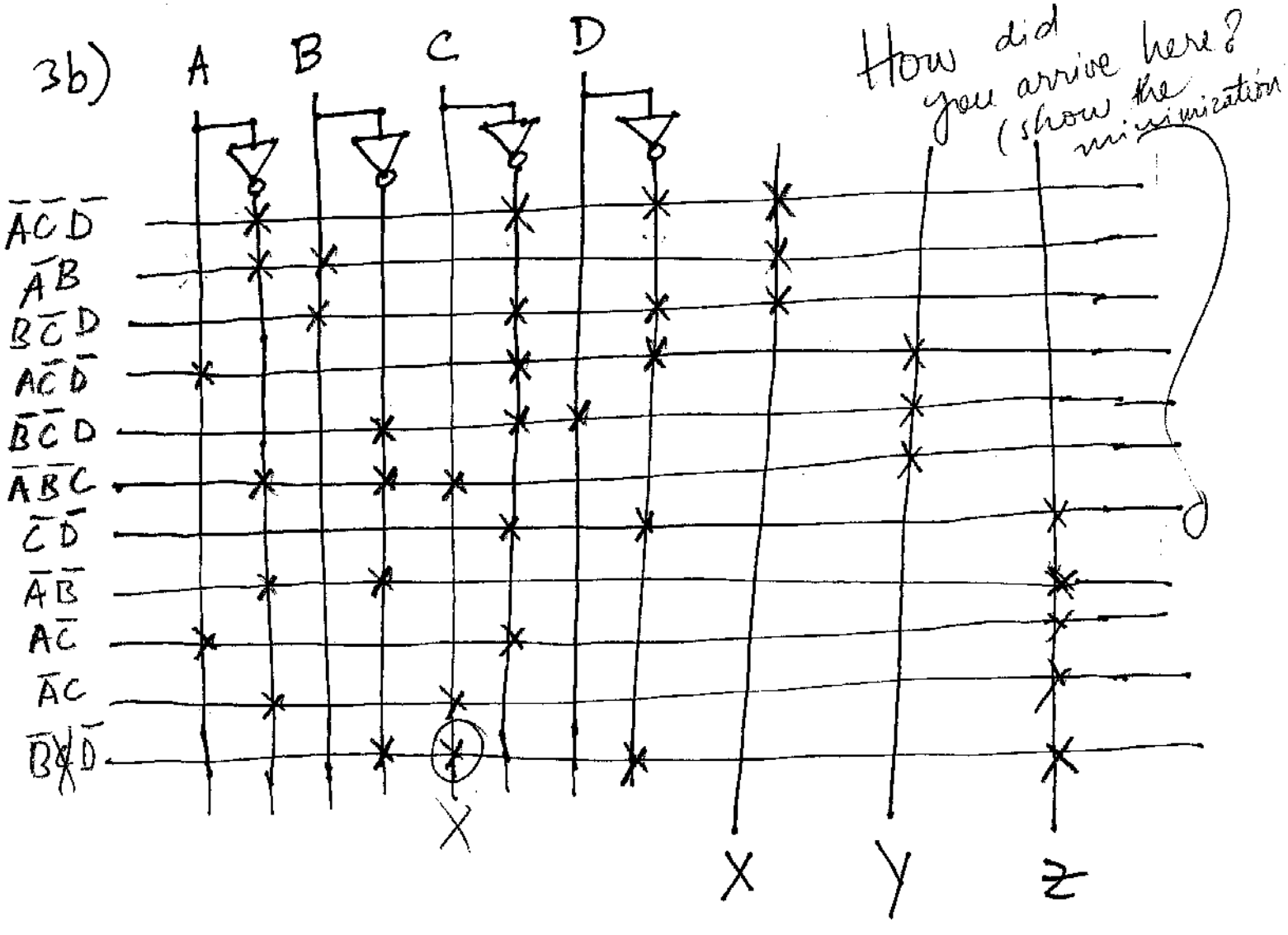
$Y = \bar{B} + AD + B$ ✓

$Z = B C \bar{C} + AD$

$= B(0) + AD$

$= AD$ ✓

3b)



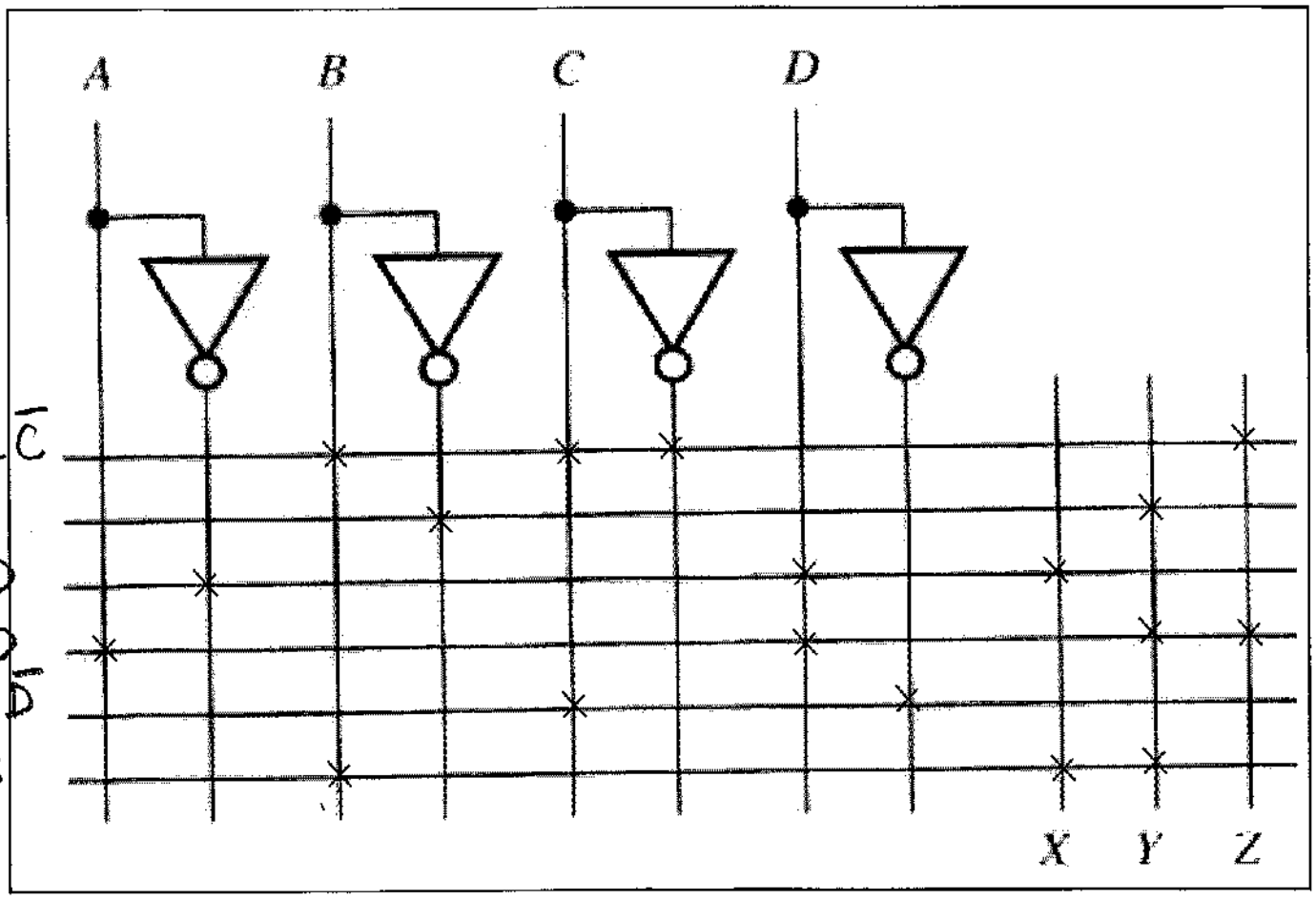


Figure 2. Programmed PLA - find the function (3.a)

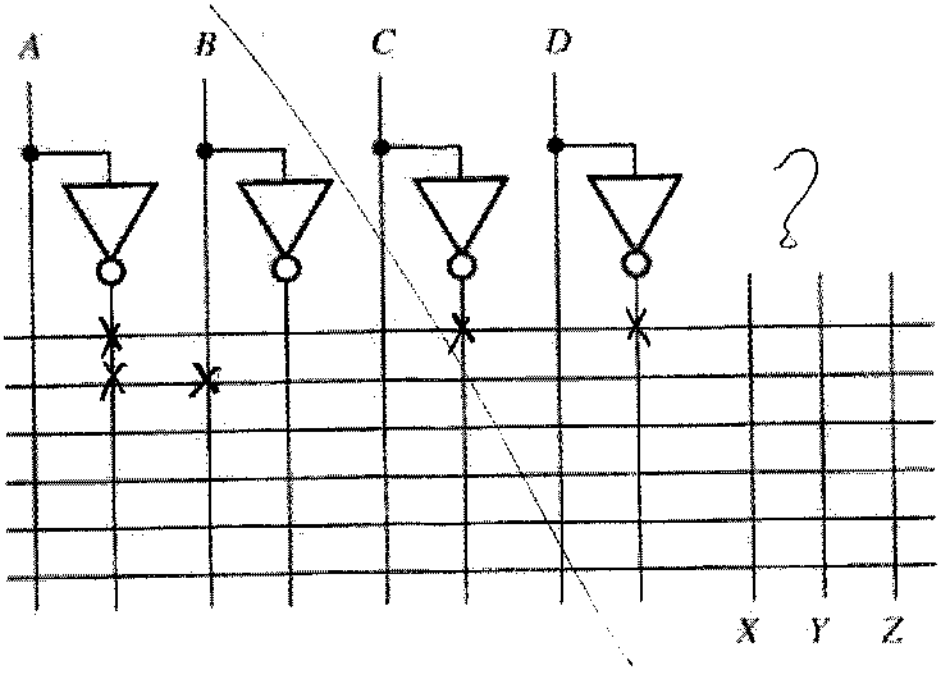
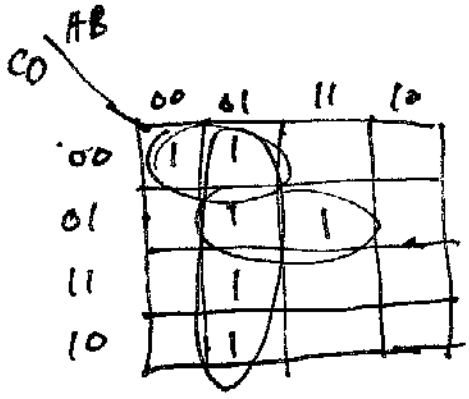


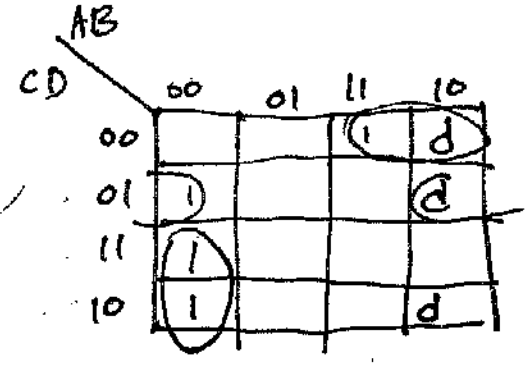
Figure 3. Blank PLA: program your functions (3.b)

36) $X_{A,B,C,D} = \sum (0,4,5,6,7,13)$



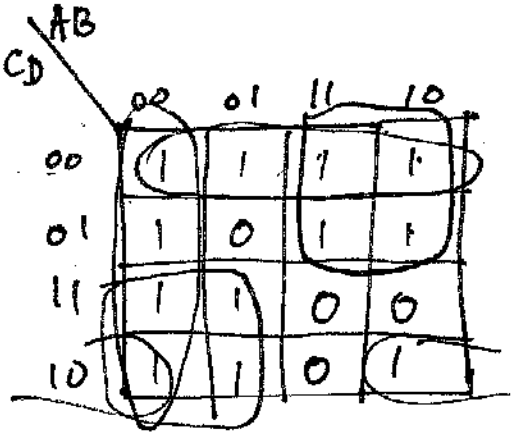
$X = \bar{A}\bar{C}\bar{D} + \bar{A}B + B\bar{C}D$

$Y_{A,B,C,D} = \sum (1,2,3,12) + d(8,9,10)$



$Y = A\bar{C}\bar{D} + \bar{B}\bar{C}D + \bar{A}\bar{B}C$

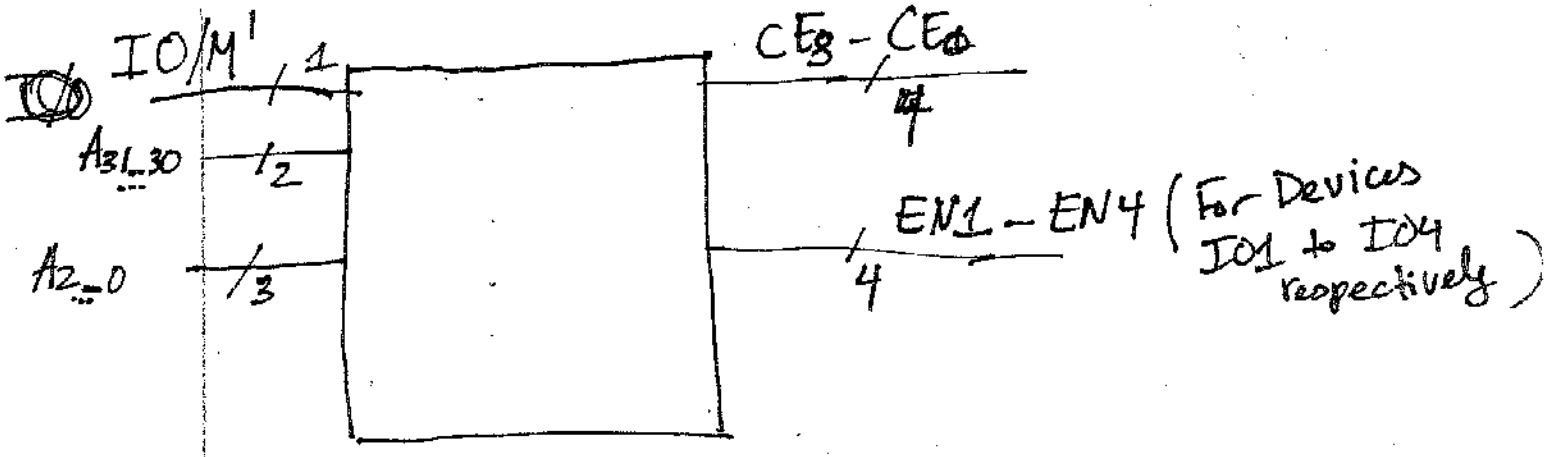
$Z_{A,B,C,D} = \prod (5,11,14,15)$



$Z = \bar{C}\bar{D} + \bar{A}\bar{B} + A\bar{C} + \bar{A}C + \bar{B}\bar{D}$

$\bar{B}\bar{D}$

Top-Level Interface (Enable signals for modules 0 to 3 respectively)



Memory Modules: Signal IO/M' = '0' (Enabled)

Truth table.

IO/M	A31	A30	CE3	CE2	CE1	CE0
0	0	0	1	1	1	0
0	0	1	1	1	0	1
0	1	0	1	0	1	1
0	1	1	0	1	1	1

$\overline{CE_0} = \overline{IO/M} \cdot \overline{A_{31}} \cdot \overline{A_{30}}$

gotta implement this !!!

The objective is to have because $\overline{CE_3}$ of the AND

IO/M	A31	A30	CE3	CE2	CE1	CE0
1	0	0	1	1	1	1
1	0	1	1	1	1	1
1	1	0	1	1	1	1
1	1	1	1	1	1	1

no need to write the Signal table again

IO/M = 1 (Disabled)

$\overline{CE_0} = (IO/M + A_{31} + A_{30})$

or

$\overline{CE_0} = \overline{IO/M} \cdot \overline{A_{31}} \cdot \overline{A_{30}}$

use one line to indicate IO/M disabled

I/O Device

I/O M' = '1' (Enabled)

(IO1) (IO2) (IO3) (IO4)

I/O M'	A2	A1	A0	EN1	EN2	EN3	EN4	
0	0	0	0	1	1	1	1	not needed (could indicate with 1 line in table)
0	0	0	1	1	1	1	1	
0	0	1	0	1	1	1	1	
0	0	1	1	1	1	1	1	
0	1	0	0	1	1	1	1	
0	1	0	1	1	1	1	1	
0	1	1	0	1	1	1	1	
0	1	1	1	1	1	1	1	
1	0	0	0	1	0	1	1	more important
1	0	0	1	1	0	1	1	
1	0	1	0	1	0	1	1	
1	0	1	1	1	1	1	0	
1	1	0	0	1	1	0	1	
1	1	0	1	0	1	1	1	
1	1	1	0	1	1	0	1	
1	1	1	1	0	1	1	1	

$$\overline{EN_1} = I/O\overline{M} \cdot A_2 \cdot \overline{A_1} \cdot A_0 + I/O\overline{M} \cdot A_2 \cdot A_1 \cdot A_0$$

$$\overline{EN_2} = I/O\overline{M} \cdot \overline{A_2} \cdot \overline{A_1} \cdot A_0 + I/O\overline{M} \cdot \overline{A_2} \cdot \overline{A_1} \cdot A_0 + I/O\overline{M} \cdot \overline{A_2} \cdot A_1 \cdot \overline{A_0}$$

$$\overline{EN_3} = I/O\overline{M} \cdot A_2 \cdot \overline{A_1} \cdot \overline{A_0} + I/O\overline{M} \cdot A_2 \cdot A_1 \cdot \overline{A_0}$$

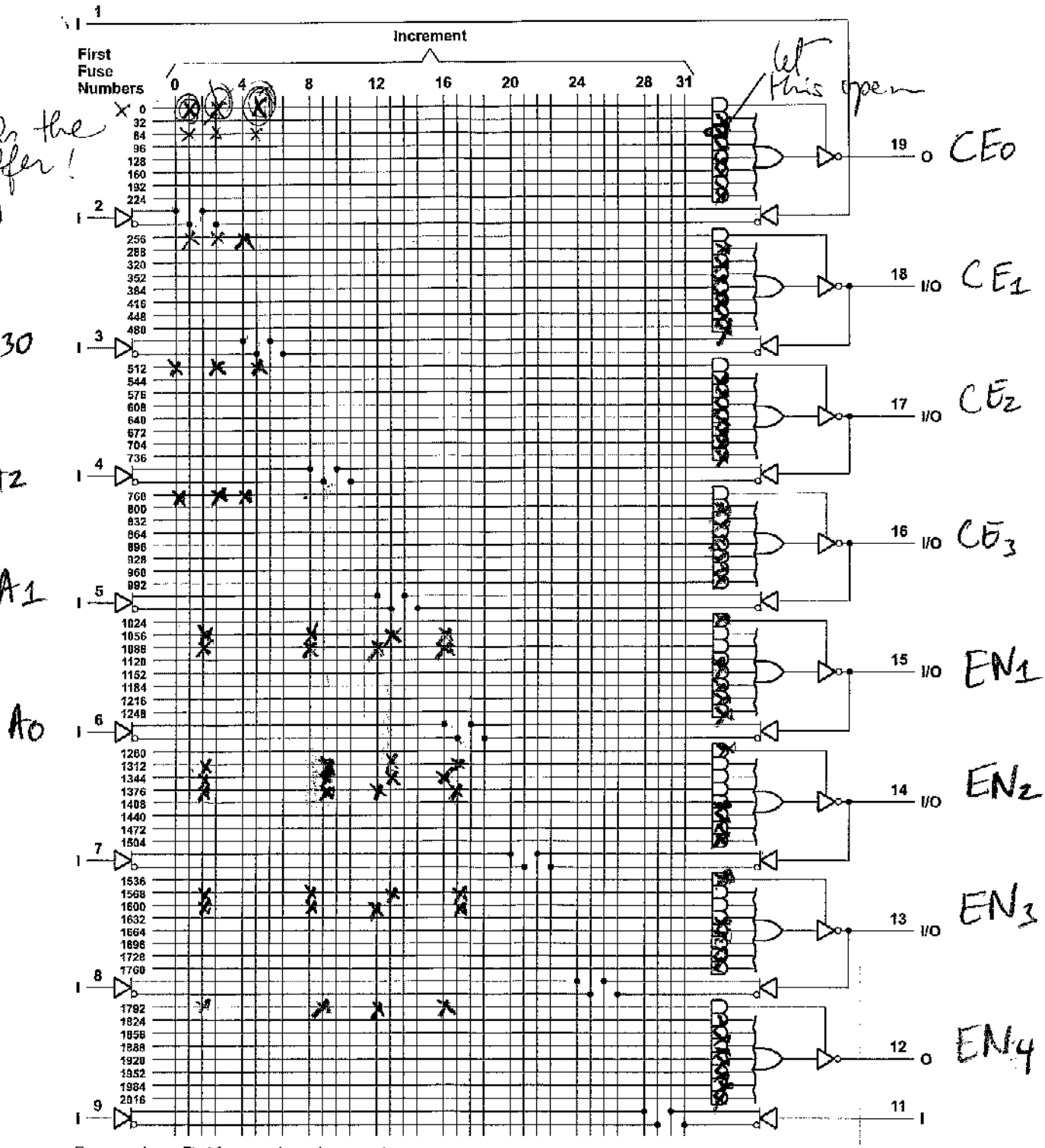
$$\overline{EN_4} = I/O\overline{M} \cdot \overline{A_2} \cdot A_1 \cdot A_0$$

$$\overline{CE_1} = \overline{I_{O/M}} \cdot \overline{A_{31}} \cdot A_{30}$$

$$\overline{CE_2} = \overline{I_{O/M}} \cdot A_{31} \cdot \overline{A_{30}}$$

$$\overline{CE_3} = \overline{I_{O/M}} \cdot A_{31} \cdot A_{30}$$

logic diagram (positive logic)



Fuse number = First fuse number + Increment