ECE 331 Digital System Design Student:_____

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HOMEWORK 9 – due **Tuesday**, November 13th at **≤6pm**

1) Feedback (3pts) – to be completed after you finish.

- F1. If you worked on it with classmates and your solutions might be TOO similar, write their names here:_____
- F2. How long did it take you to work on the homework (don't count the reading assignment!)
  1h 2h 4h infinite hours
- F3. Do you have suggestions on how to improve it? (ideas for new problems?) Let us know here (and/or use your own homework sheets):

2) SWC and SBC scenarios (20 pts)

Determine the minimum and maximum propagation delays for the two circuits below. Assume that the LS parts were supplied by ON Semiconductor, and that the Fast TTL (F) and HC parts are from Philips. Analyze both outputs using SWC and SBC techniques.

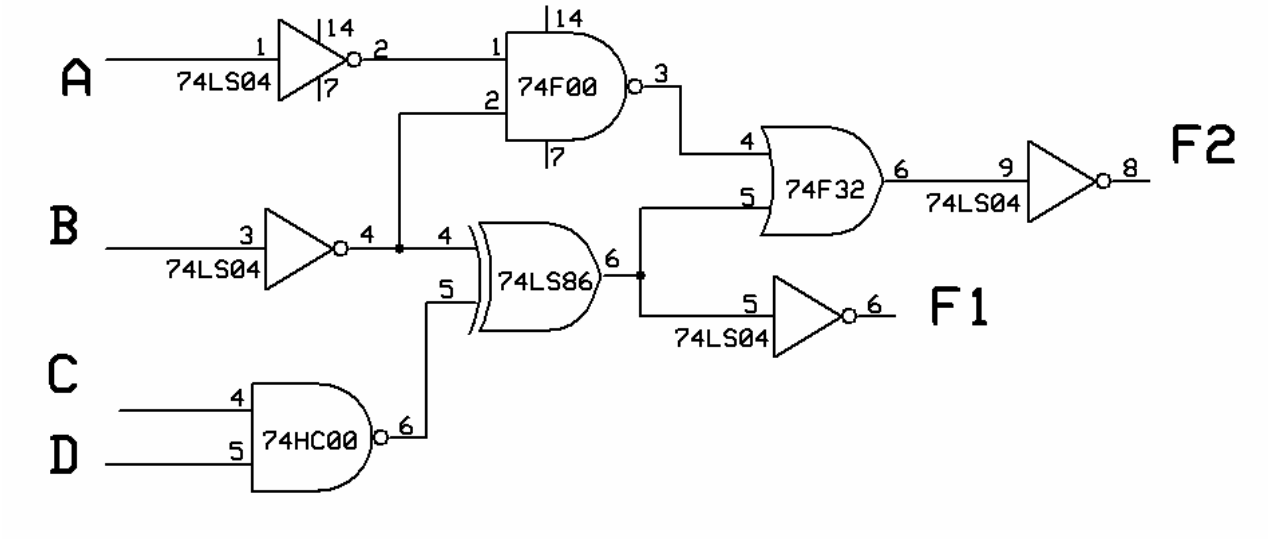

figure 1. Circuit schematic for problem 2.

3) Programming PLA devices

(a) Write the shorthand notation ($f_{A,B,C,D}=\Sigma$ (?)) the logic function associated with X, Y, and Z in figure 2. The notation used in the figure below follows the same idea as figure 3.27 in Brown's book: the horizontal lines are inputs to AND gates, and the vertical lines on X, Y, and Z are inputs to OR gates (9pts).

(b) Now use figure 3 (or copy it, or make your own) to implement the three functions described below. If needed, draw more horizontal lines (21 pts).

$$X_{A,B,C,D}=\Sigma\ (0, 4, 5, 6, 7, 13);$$
$$Y_{A,B,C,D}=\Sigma\ (1,2,3,12)+d(8,9,10);$$
$$Z_{A,B,C,D}=\Pi\ (5,11,14,15);$$

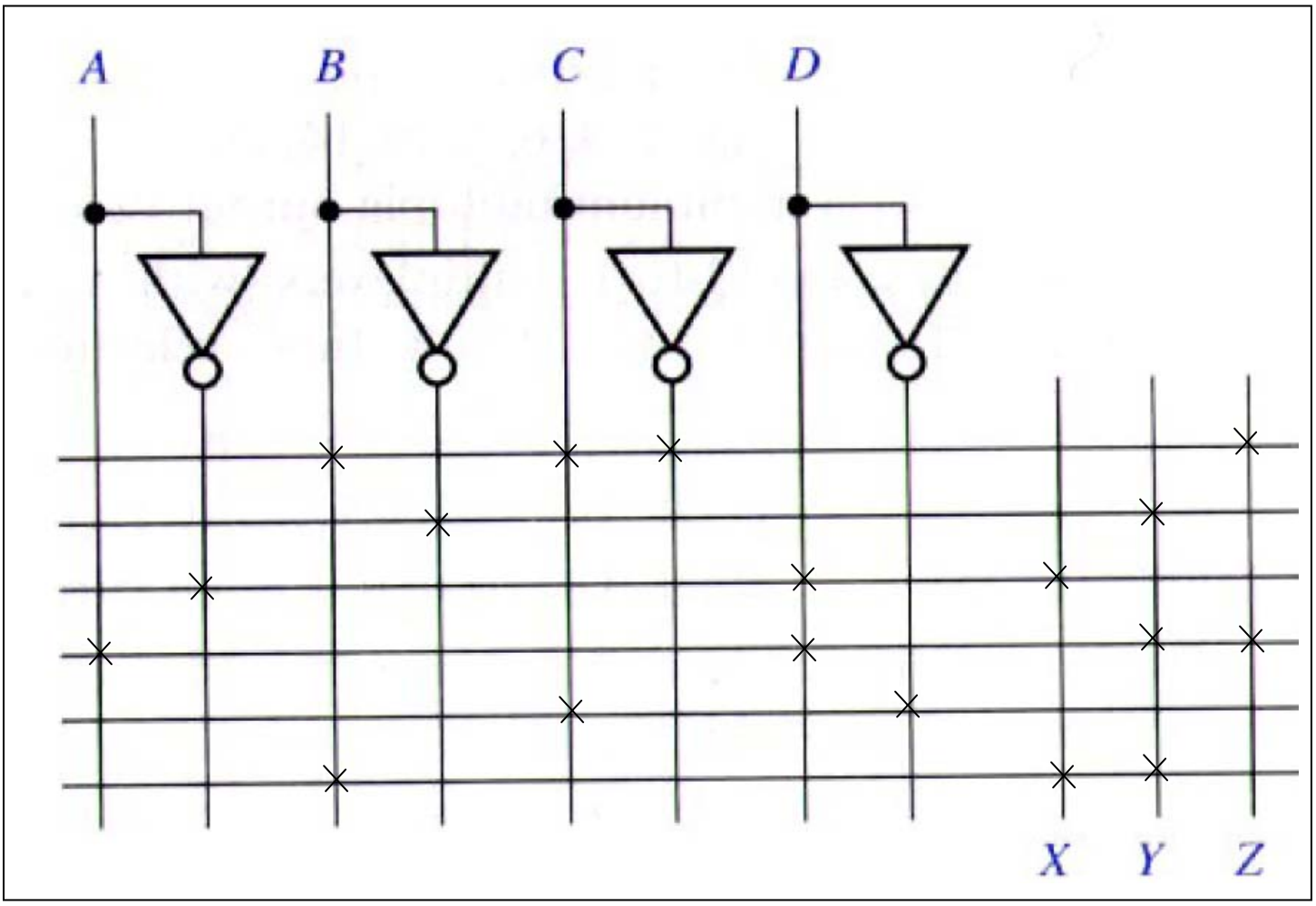

Figure 2. Programmed PLA – find the function (3.a)

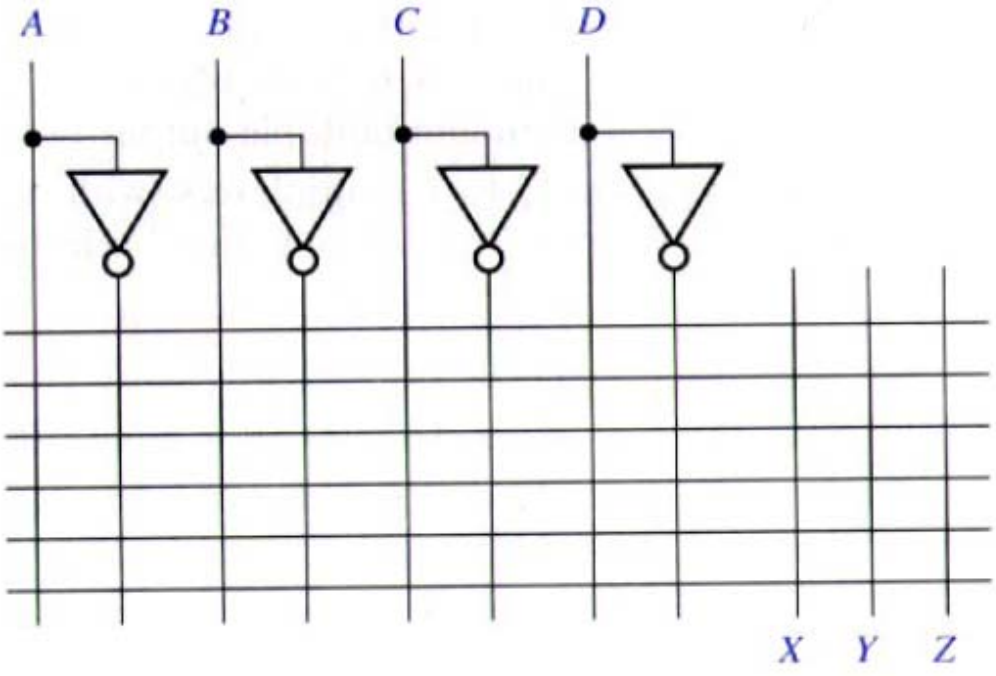

Figure 3. Blank PLA: program your functions (3.b)

4) Digital System Design with commercial PAL (47 pts)

We are designing a simple computer with a 32-bit long address bus. You should design part of the address decoder for it. The decoder determined whether the address selects a memory module or an I/O (input/output) device.
Details to be considered in your project are:
- Signal IO/M' (output from your decoder) is set to '1' if the address is meant for an IO device, and '0' for a memory module.
The project can be broken down in two sets, one for memory, and one for IO:

- Two MSBs of the address (A_{31} and A_{30}) generate enable signals for four memory modules. The memory modules have low active enable lines CE_0' through CE_3' for modules 0 through 3, respectively. (So in the design we have to select module 3 when A_{31}=A_{30}=1, for example.)
- The IO devices are selected through the three LSBs (A_2, A_1, and A_0). We have four devices, one through four (IO1 – IO4), with EN1' through EN4' active low enables. Each one of these devices should be enabled for the following addresses:
    - IO1 for addresses 5 and 7,
    - IO2 for addresses from 0 through 2,
    - IO3 for addresses 4 and 6,
    - IO4 for address 3.

In this case, the pin IO/M' is set to '1' (indicating the selection of an IO device.)

Design the decoder as you have done many other designs (it is the same process!). After designing it, implement your SOP design using the PAL16L8AM, by Texas Instruments. Use page 5 from the datasheet (available online at: http://focus.ti.com/lit/ds/symlink/pal16l8am.pdf).

Tip:
- Do not use all the 32 bits of the address bus. Make it simple. Follow the steps for system design.
- IO/M' is an input too.
- Read the PAL16L8 datasheet (scan it); in particular notice that the outputs are active low (and thus match with the requirements of this design).