HWK # 7

② Decoders always enabled and $\overline{G2A}$, $\overline{G2B}$ from 74138 grounded. $\overline{G1}$, $\overline{G2}$ and D from 74154 also grounded. Outputs active low for both chips.

D74138

C	B	A	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
0	0	0	0	1	1	1	1	1	1	1
0	0	1	1	0	1	1	1	1	1	1
0	1	0	1	1	0	1	1	1	1	1
0	1	1	1	1	1	0	1	1	1	1
1	0	0	1	1	1	1	0	1	1	1
1	0	1	1	1	1	1	1	0	1	1
1	1	0	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	1	0

D74138

C	B	A
1	1	1
1	1	1
1	0	0
1	1	1
1	1	1
1	1	1
0	1	1
1	1	1

D74154

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1
1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1

$G = \overline{Y_0 \cdot \overline{1}\text{ (pin)}}$

$M = \overline{\overline{0}\text{ (pin)}}$

$U = \overline{3}\text{ (pin)} \oplus \overline{12}\text{ (pin)}$

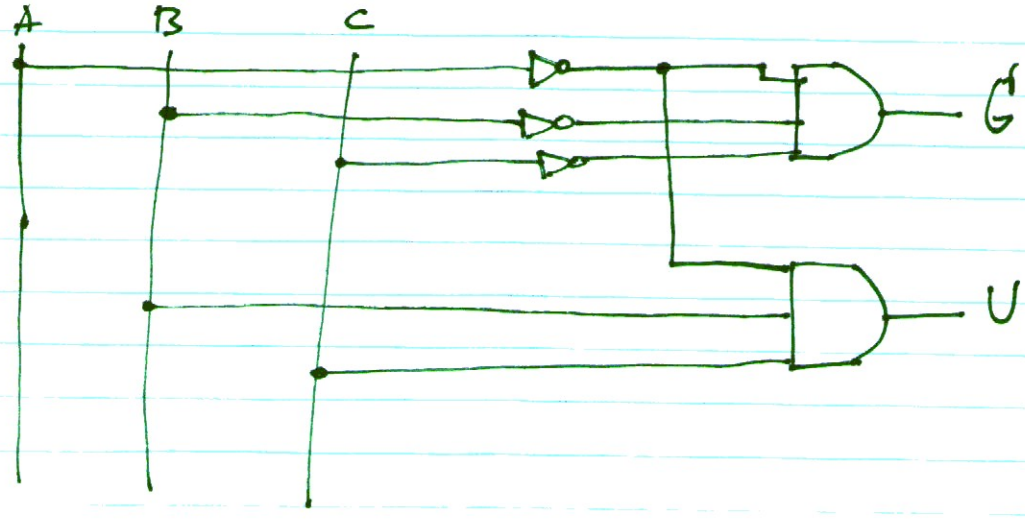
Pins from D74154

G	M	U
1	0	0
0	0	0
0	0	0
0	0	0
0	0	0
0	0	0
0	0	1
0	0	0

$G = \bar{A}\bar{B}\bar{C}$

M = No Minterms

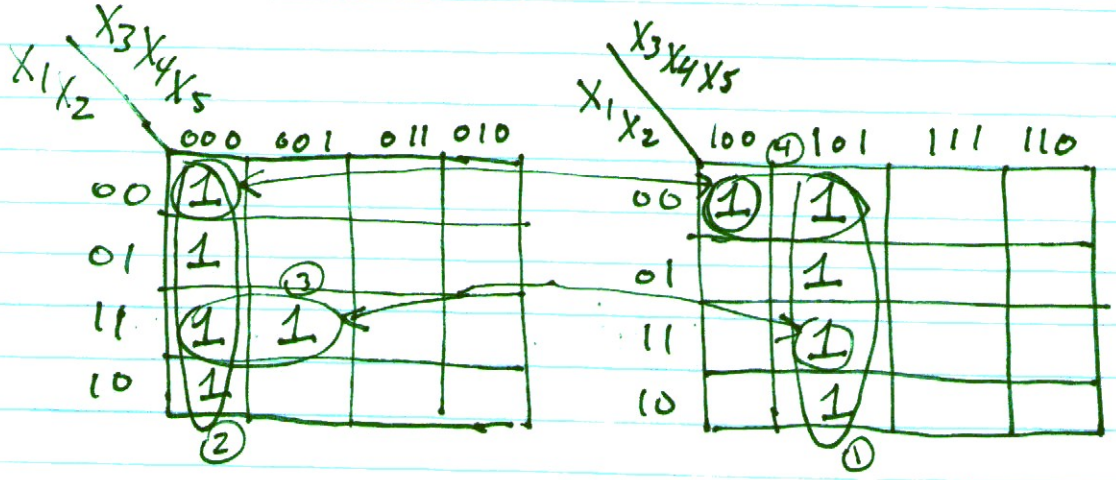
$U = \bar{A}BC$



(3)

a) $f(X_1, X_2, X_3, X_4, X_5) = \Sigma\, 0,4,5,24,25,29 + d\,(8,13,16,21)$

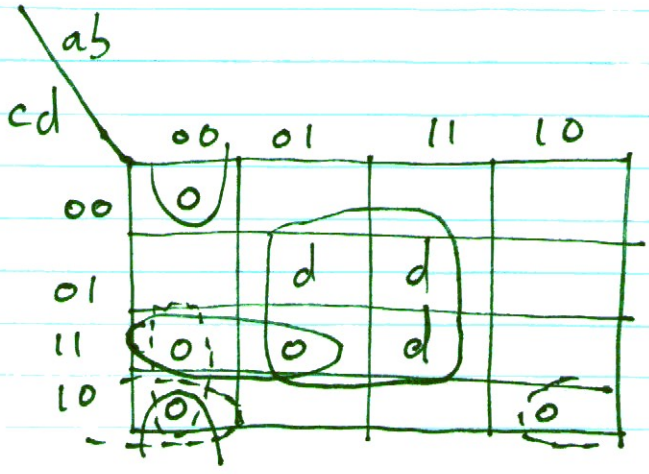
	X_1	X_2	X_3	X_4	X_5	
0	0	0	0	0	0	
4	0	0	1	0	0	
5	0	0	1	0	1	
24	1	1	0	0	0	
25	1	1	0	0	1	
29	1	1	1	0	1	
8	0	1	0	0	0	(d)
13	0	1	1	0	1	(d)
16	1	0	0	0	0	(d)
21	1	0	1	0	1	(d)



$$F = X_3 \bar{X_4} X_5 + \bar{X_3} \bar{X_4} \bar{X_5} + X_1 X_2 \bar{X_4} + \bar{X_1} \bar{X_2} \bar{X_4}$$

b)

$$g(a,b,c,d) = \Pi(0,3,2,7,10) + d(5,13,15)$$



$$g = (a + b + d)(b + \bar{c} + d)(a + \bar{c} + \bar{d})$$
$$(\bar{b} + \bar{d})(a + b + \bar{c})$$

4) Yes it is possible for this circuit to present static hazards that in turn can cause dynamic hazards.

Because of the propagation delay impossed by NAND2 on the circuit diagram, the first input (1) on the OR gate may update faster than the second input. Also the 3-input AND gate 7411 may have a greater propagation delay than the two input nand gate. On either case output G may have a momentary incorrect output value due to these delays caused by the gates.

5)

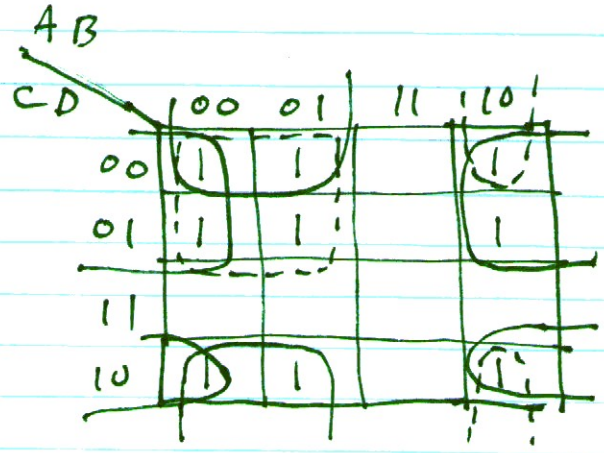
a)

2	NAND (2-input)	=	2	x 4	=	8
1	AND (3-input)	=	1	x 8	=	8 +
1	OR (2-input)	=	1	x 6	=	6
						22

transistors

5b)

A	B	C	D	1	2	3	4	5	6	7	8	F
0	0	0	0	0	1	0	1	0	1	0	1	1
0	0	0	1	0	1	0	1	0	1	1	0	1
0	0	1	0	0	1	0	1	1	0	0	1	1
0	0	1	1	0	1	0	1	1	0	1	0	0
0	1	0	0	0	1	1	0	0	1	0	1	1
0	1	0	1	0	1	1	0	0	1	1	0	1
0	1	1	0	0	1	1	0	1	0	0	1	1
0	1	1	1	0	1	1	0	1	0	1	0	0
1	0	0	0	1	0	0	1	0	1	0	1	1
1	0	0	1	1	0	0	1	0	1	1	0	1
1	0	1	0	1	0	0	1	1	0	0	1	1
1	0	1	1	1	0	0	1	1	0	1	0	0
1	1	0	0	1	0	1	0	0	1	0	1	0
1	1	0	1	1	0	1	0	0	1	1	0	0
1	1	1	0	1	0	1	0	1	0	0	1	0
1	1	1	1	1	0	1	0	1	0	1	0	0

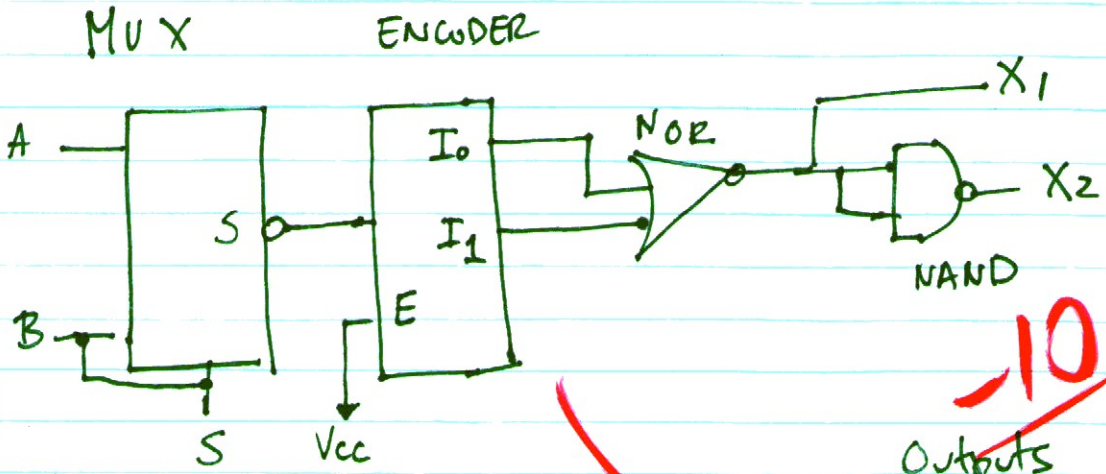


$$F = \bar{A}\bar{C} + A\bar{D} + \bar{B}\bar{C} + A\bar{B}\bar{D} + \bar{B}C\bar{D}$$

6) EXTRA CREDIT

MANY WAYS TO DO THIS.

ONE EXAMPLE FROM A STUDENT



-10

INPUTS A	B	S	I_0	I_1	Outputs X_1	X_2
0	0	0	0	1	1	0
0	1	1	1	0	1	0
1	0	1	1	0	1	0
1	1	1	1	0	1	0

X1 is ALWAYS 1,
X2 is ALWAYS 0.

The question states that output cannot be like that.

X_1 & X_2 Never equal to $X_1 = 0$ & $X_2 = 0$ or $X_1 = 1$ & $X_2 = 1$ For all 4 combination of inputs of A, B.

This answer would NOT qualify for extra credit.