ECE 331 Digital System Design Student:_____

Fall 2007 Nathalia Peixoto

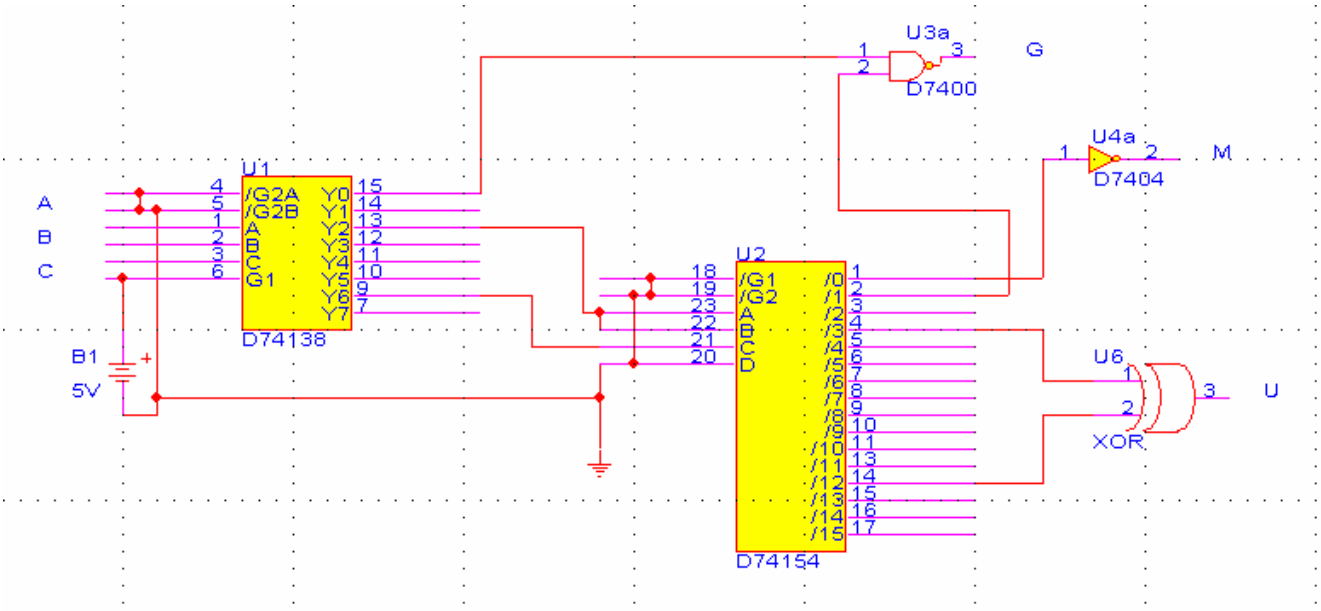
HOMEWORK 7 – due **Tuesday**, October 30th at **≤6pm**

1) Feedback (3pts) – to be completed after you finish.

- F1. If you worked on it with classmates and your solutions might be TOO similar, write their names here:_____
- F2. How long did it take you to work on the homework (don't count the reading assignment!)
  2h 4h 6h 8h 10h infinite hours
- F3. Do you have suggestions on how to improve it? (ideas for new exercises?) Let us know here (and/or use your own homework sheets):

2) Review (decoders)

(a) Present a truth table with the outputs G, M, and U as a function of the inputs (A,B, and C, connected to the inputs of the 74138). Assume all ICs are powered appropriately, and that the decoders are the ones actually depicted in the schematic (that is, 74138 and 75154). (17 pts)



(b) Design a hazard-free minimized logic circuit which performs the same function as the circuit above. (10 pts)

3) Hazard (25 pts)

(a) Find a hazard-free minimum cost implementation of the function:

$$f(x1,x2,x3,x4,x5)= \sum 0, 4, 5, 24, 25, 29+d(8, 13, 16, 21)$$

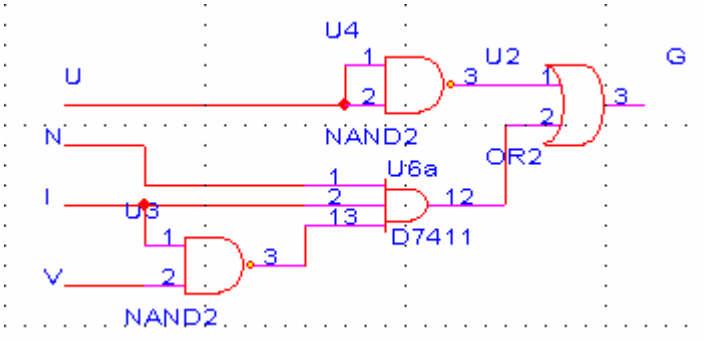
Obs. I am expecting you to solve this with K-maps (two 4-var K-maps side by side).

(b) Find a hazard-free minimum cost implementation of the function:

$$g(a,b,c,d)=\pi 0, 2, 3, 7, 10 + d(5, 13, 15)$$

4) Hazard analysis (15 pts)

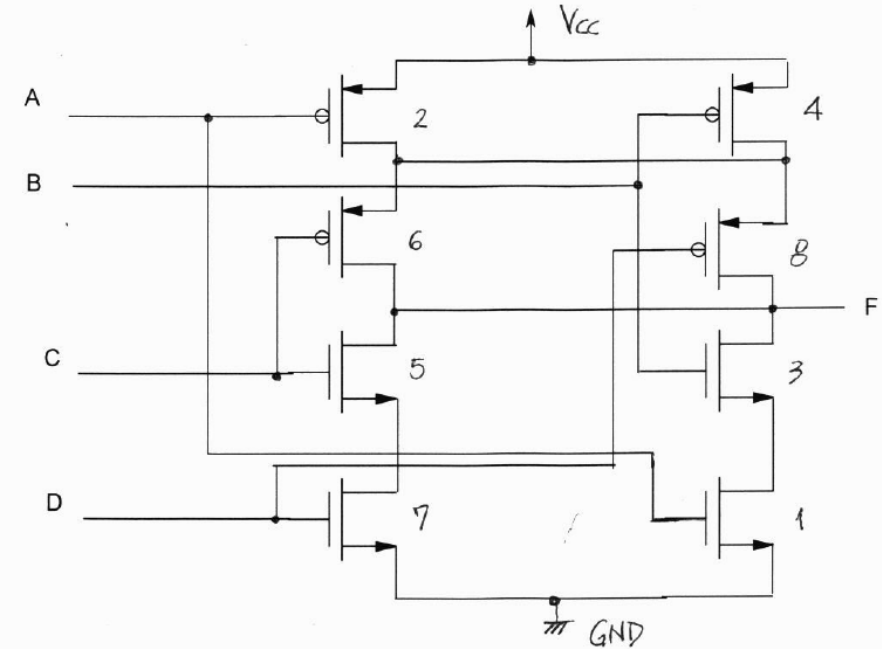
Does this circuit present any static or dynamic hazards? (Yes/No answers are not acceptable: show how you got to the conclusion!)



5) CMOS

(5 pts) (a) How many transistors are needed to implement the **previous** circuit in CMOS technology?

(15 pts) (b) Write a function table for the circuit below.



(10 pts) (c) Using the function table from 5b, derive the logic function, minimize it, and implement a minimal circuit to execute the same function.

6) Extra credit (10pts: either 10 or 0).

Use priority encoders or decoders (up to 8 lines of input/output), NOR, NAND, or AND gates, and muxes/demuxes (up to 8 lines again) to come up with a circuit with 2 inputs and two outputs, which does not yield all "0"s nor all "1"s in the outputs. Your restrictions are: minimum of one mux (or demux), minimum of one encoder (or decoder), minimum of two logic gates, and maximum of 4 logic gates. At least one of the integrated circuits has to run active low lines (either inputs or outputs, or both). Show the circuit and the function table with all (as many as possible) states of internal lines (not only inputs and outputs). If you only show the answers, you receive zero for the extra credit. (There are no partial points here!) Tip: look at the midterm: question #10 would be a possible answer to this problem. (Please do NOT copy it – you are supposed to come up with your own original circuit!)