

HOMEWORK 6 - due **Thursday**, October 11<sup>th</sup> at **≤6pm** 

## 1) Feedback (3pts) - to be completed after you finish.

- F1. If you worked on it with classmates and your solutions might be TOO similar, write their names here:\_\_\_\_\_\_
- F2. How long did it take you to work on the homework (don't count the reading assignment!) 2h 4h 6h 8h 10h infinite hours
- F3. Do you have suggestions on how to improve it? (ideas for new exercises?) Let us know here (and/or use your own homework sheets):

# 2) Adders

The circuit below performs addition and subtraction. FA stands for full adder.

(a) Write the values of C4, S3, S2, S1, and S0, for the four cases shown in the table. A and B are 4 bit inputs, S is the input select.



s	$A_3A_2A_1A_0$	$B_3B_2B_1B_0$	$C_4$	$\mathbf{S}_3$	$S_2$	$\mathbf{S}_1$	$S_0$
0	1011	0111					
1	1100	0011					
1	0101	1000					
0	0100	1100					

b) Implement a circuit to detect overflow. If you are not clear on how to do that, first review your notes. (Or homework 4, # 5, or homework 5, # 3). Tip: follow the digital system design steps you learned in class.

#### 3) Encoders/ decoders/ multiplexers

Hint: You can use boolean algebra for question a) and a function table with columns for all inputs and for all outputs of all devices for question b).

a) Find a simplified Boolean equation for output G below. Each box below represents a multiplexer, with inputs A and B and control input S (S=0 selects input A):



b) Find a simplified Boolean equation for output G below:



#### 4) (de)Multiplexers

Design a 1-to-4 demux. Follow the logic circuit design steps discussed in class.

### 5) VHDL

Write the entity and architecture for a 1-to-8 demux.

#### 6) Extra credit

Fill out the following table with 0's and 1's (0 for false, 1 for true):

	74hct42	Sn74lvc1g18	74hc4511
1. This chip has active low signals.			
2. It can only be used as demux.			
3. It can only be used as decoder.			
4. It can be used as either decoder or demux.			
5. It costs more than one dollar.			