*ECE 331 Digital System Design* Student:_____

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# HOMEWORK 12 – due **Tuesday**, December 4th at **≤6pm**

## 1) Feedback (3pts) -complete after you finish.

- F1. If you worked on it with classmates and your solutions might be TOO similar, write their names here:_____
- F2. How long did it take you to work on the homework (don't count the reading assignment!)
  1h 2h 4h infinite hours
- F3. Do you have suggestions on how to improve it? (ideas for new problems?) Let us know here (and/or use your own homework sheets):

*Obs: I know this is a not very challenging homework. It only refers to one class (not to two!). If you are disappointed, please let me know. I will upload more interesting problems in the next two weeks, for the "final 331 challenge".*

## 2) State diagrams

(a) For the state/output table below, give the state transition table, using 1-hot encoding (5 pts).

(b) Draw the state diagram (4 pts)

(c) How many states are unused? (3 pts)

(d) Is this a Mealy or Moore machine, and why? (5 pts)

| State | X=0 | X=1 | X=0 | X=1 |
|---|---|---|---|---|
| a | b | c | 1 | 1 |
| b | a | c | 0 | 0 |
| c | c | c | 1 | 1 |

Table 1. State/output table for problem 2. First column refers to current state. Second and third columns refer to next state. Last two columns refer to output. X is the input.

## 3) State minimization (20 pts)

Minimize the state diagram below by finding the equivalent states. Draw the minimized state machine.

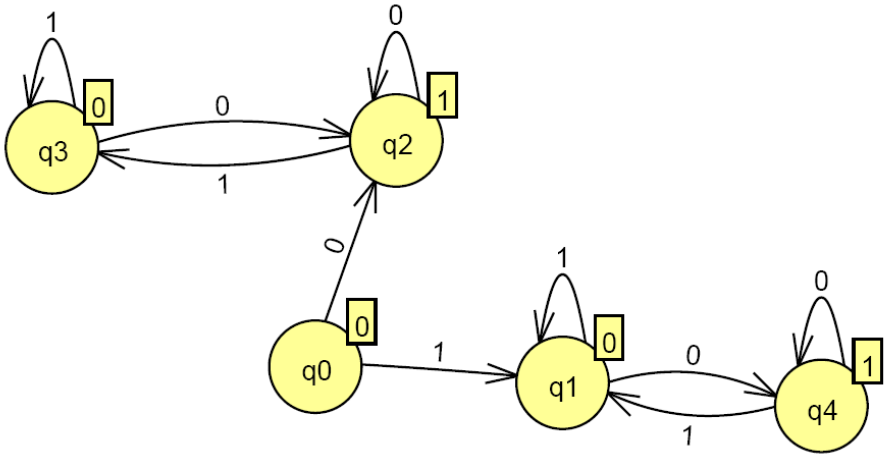


Figure 1. State machine. States go from q0 through q4, outputs are shown in the same color as states (in squares on the upper right corner of states). Inputs are shown on top of arrows, as usual in a Moore machine.

## 4) State machine design

Consider a Moore machine that outputs the sequence 0,1,3,0,1,3,… if its single input, *D* = 1, and the reversed sequence (i.e. 3,1,0,3,1,0,*: : :*) if *D* = 0. The *D* can change between any two clock pulses, and the reversal starts on the next clock pulse. So if *D* changes from 1 to 0 when the output of the state machine is 3, the next output will be 1.

(a) Draw the state diagram (15 pts)

(b) Minimize your states, and present a transition table with minimal state assignment (15 pts)

## 5) State machine analysis

(a) Complete the modified state transition table given below. This circuit has two flip-flops: T with enable (input signal identified below as EN, for Q0), and a JK (with input signals identified here as J1 K1). Note that the table has already the state assignment and the value of the next state, as well as the output, set. (15pts)

| **Current state** | **Next state** | | **Output (w)** | | **EN (T f-f)** | | **J1K1** | **J1K1** |
|---|---|---|---|---|---|---|---|---|
| **Q0Q1** | **X=0** | **X=1** | **X=0** | **X=1** | **X=0** | **X=1** | **X=0** | **X=1** |
| | **$Q0^+Q1^+$** | **$Q0^+Q1^+$** | | | | | | |
| 0 0 | 1 0 | 0 1 | 0 | 0 | | | | |
| 0 1 | 0 1 | 0 1 | 1 | 0 | | | | |
| 1 0 | 0 0 | 0 0 | 0 | 0 | | | | |
| 1 1 | 1 1 | 0 0 | 1 | 1 | | | | |

Table 2. Modified state transition table for problem 5

(b) Show the state diagram for this state machine (15 pts)