ECE 331 Digital System Design Student:_____

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HOMEWORK 11 – due **Tuesday**, November 27th at ≤**6pm**

1) Feedback (3pts) -complete after you finish.

- F1. If you worked on it with classmates and your solutions might be TOO similar, write their names here:_____
- F2. How long did it take you to work on the homework (don't count the reading assignment!)
  1h 2h 4h infinite hours
- F3. Do you have suggestions on how to improve it? (ideas for new problems?) Let us know here (and/or use your own homework sheets):

2) Flip-flops

(a) Using D-flip-flops, design a counter that shows the following sequence in the output line (G): 0, 2, 1, 3 (then it goes back to the beginning). (10 pts)

(b) Now implement the same circuit using JK flip-flops. (7 pts)

3) State machine analysis

(a) Analyze the circuit below, following the steps shown in class. Note that, because there is an input, the state diagram table will have 10 columns. (15 pts)

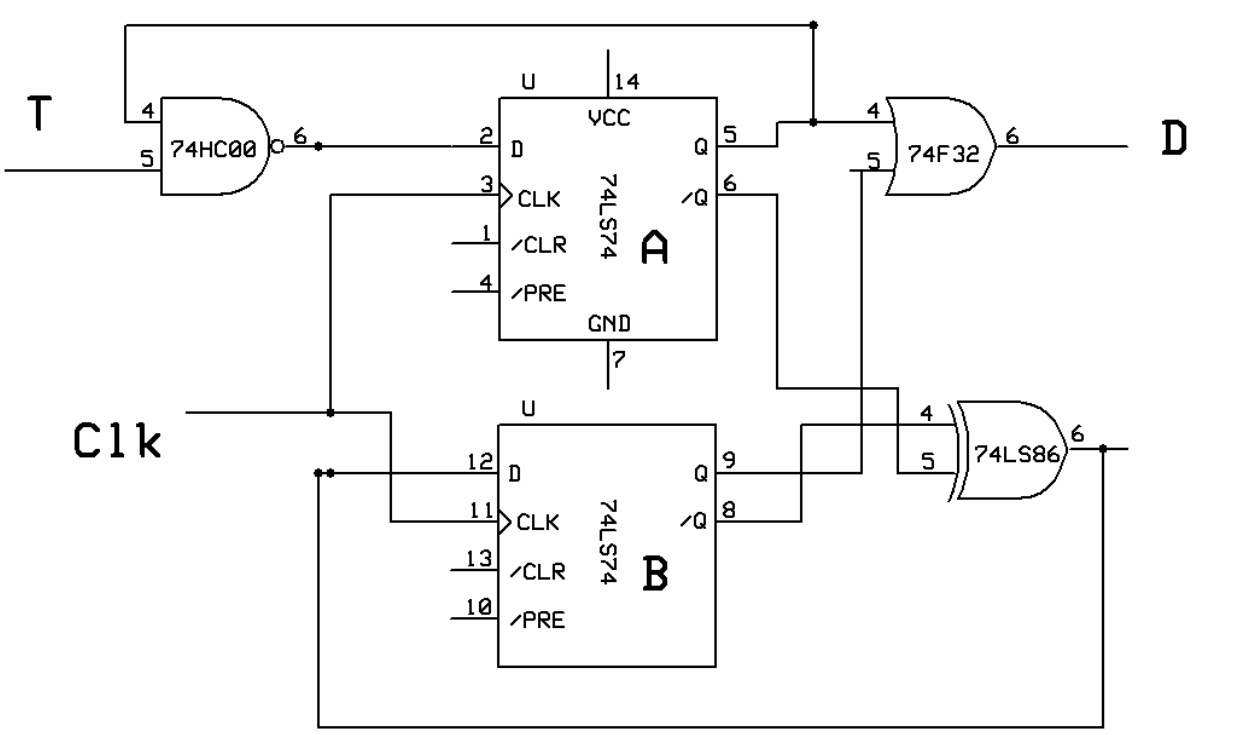

Figure 1. Circuit for problem 3a. Assume that the clear and preset lines, as well as the power for all ICs, are wired "right" – that is, both flip-flops are enabled, and all ICs powered. This circuit has only one output: D.

(b) Analyze the circuit from figure 2, following the steps shown in class. (15 pts)

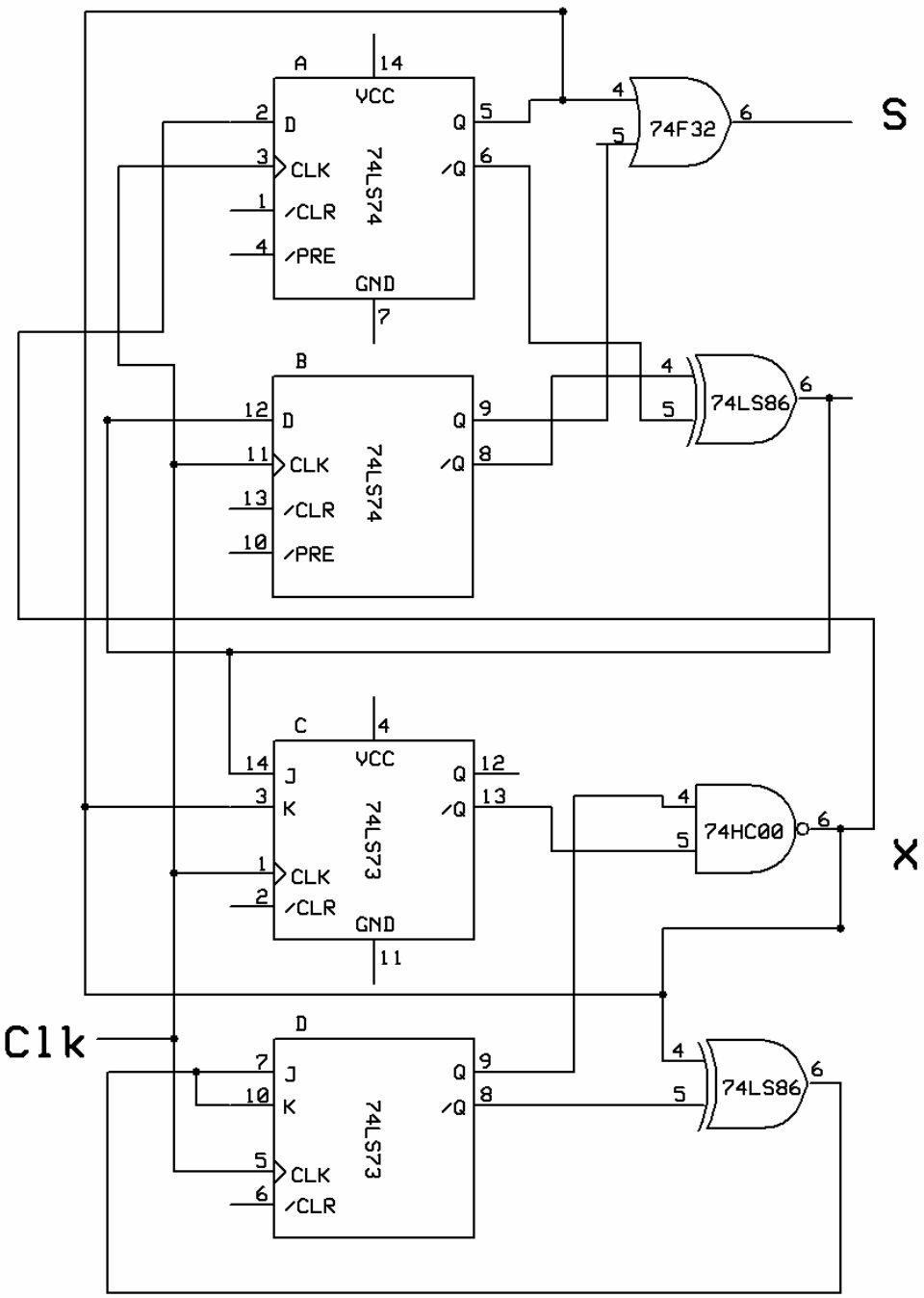

Figure 2. State machine analysis, problem 3b. Note that the identification of each flip-flop is on the upper right corner (they go from A to D). Flip-flops C and D are of type JK (so before you write the state equations make sure you remember how they work. For D flip-flops, we write $Q^+=D$. Look up the equations for JK and T. Assume all ICs are properly powered, the clock is working, and the CLR and PRE lines are not active (that is, all flip-flops are enabled and functional).

4) State machine design.

(a)Design a state machine with an input (Y) and output (P). It generates a valid output (1) when it detects one of two words: 1100 or 1001. Allow overlap. That is, 1001001 would generate two "1"s (for this particular input sequence, the output would be 0001001. (25pts)

(a) Write the VHDL code for your state machine. While we haven't explicitly talked about this in class, you should have done this in the lab, seen it in the recitation, and the book shows examples in pages 567-568. (5pts)

5) Shift registers (20 pts)

Figure 3 shows a cyclic shift register (there are many many types of such CSRs). What sequence of states does it step through, if the initial conditions are all Q's=0, when the clock ticks?

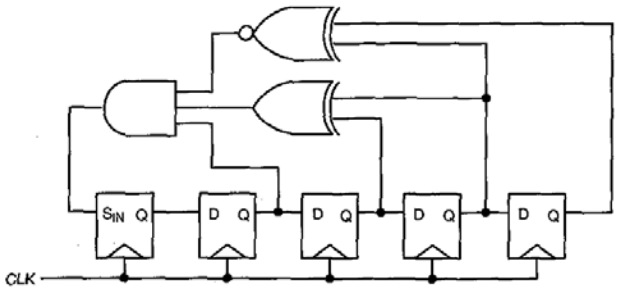

Figure 3. Shift register for problem 5. Assume the first ff (with Sin) is A, and then B, C, D, and E.

6) Extra special credit (50 pts). Yes, 50 pts. I strongly advise you to think about this problem.

Consider a 4-by-4 matrix keyboard (figure 4). When a button is pressed, a row wire and column wire are connected together, otherwise no wires touch. You task is to decode the keyboard, that is, have a four-bit word representing a particular button be presented by the system as long as that button is pushed. You can only use the following ICs:

A 4-to-1 mux; a 2-to-4 decoder; a 4-bit synchronous binary counter (74LS169); a function generator set to a square wave at 1KHz with the right offset (to be used as the clock); an LCD display with four inputs for data (hexadecimal values) and an active high blanking input (BL): when that line is "0", nothing is displayed.

First connect the pulse generator to the counter, and let the counter output represent the button pushed. How should the MUX and decoder be connected to the counter and the keyboard to finish the job? Should the R's and C's be input or output?

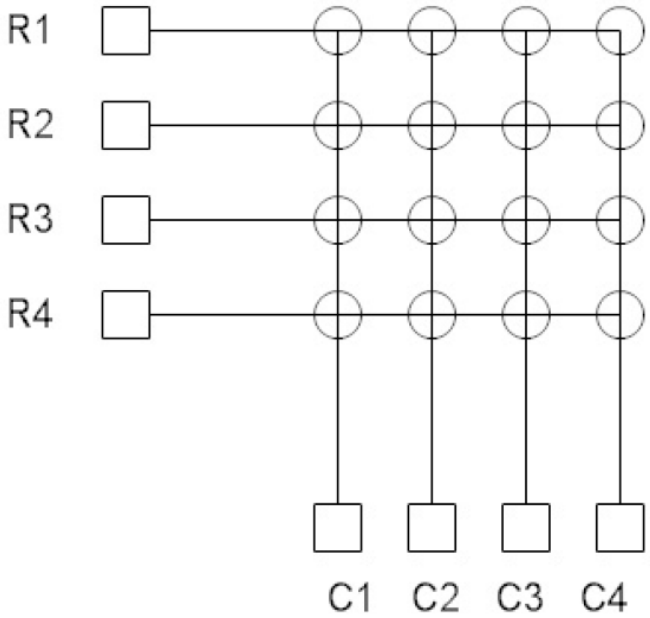

Figure 4. 16-key keyboard.

PS – At the time of "printing", I have only sketched out my ideas to solve this problem (which don't involve any other ICs). You may need one or a couple of logic gates to fully comply with the requirements of the problem (but if you don't it's even better: that's the objective!)