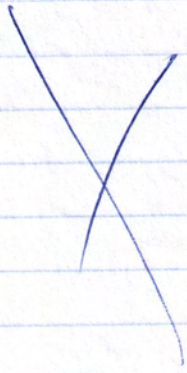
HWK # 10

2a) Truth Table

A	B	C	Y_1	Y_2	Y_3
0	0	0	1	1	1
0	0	1	1	1	0
0	1	0	1	0	1
0	1	1	1	0	1
1	0	0	0	1	1
1	0	1	0	1	1
1	1	0	0	1	1
1	1	1	0	1	1



States ~~0 1 X~~ ~~1 X X~~ are stable

110, 101, 011 Are stable

~~X~~ Not Allowed Inputs A=0, B=0, C=0

what's behind it:

- Given that ONE output is "0", that line forces the other two outputs to go to "1".
- In none of the other rows you can reason like that.

In particular for A=B=C=1 there is no definition of state (other than $Y_i{}^+ = Y_i$ if stable).

3a) ✓

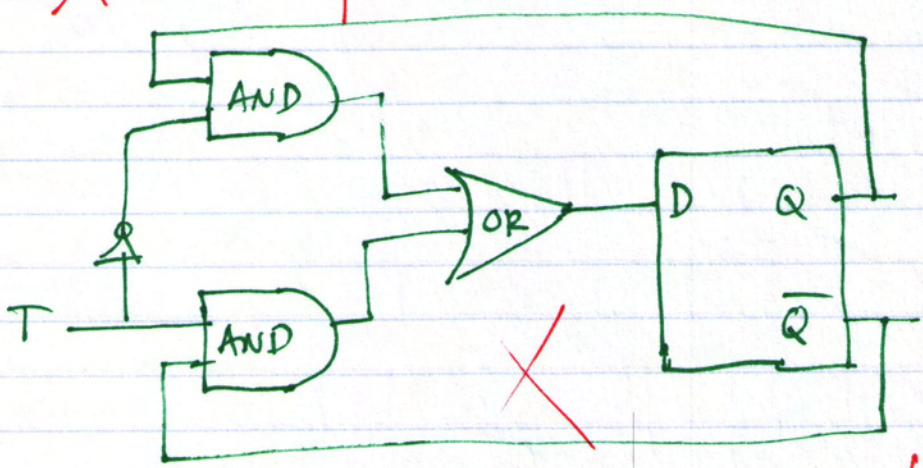
	Clk	Q_2	Q_1	Q_0
t_0		0	0	0
t_1	↑	0	0	1
t_2	↑	0	1	0
t_3	↑	1	1	1
t_4	↑	0	0	0
t_5	↑	0	0	1

Counter Sequence:
000, 001, 010, 111

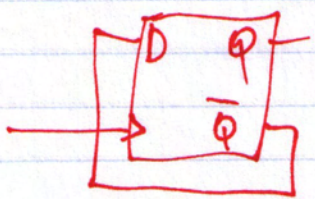
Yes, it counts
000, 001, 010, 111, 000.

3b) T-Flip Flop using D-flip-flop:

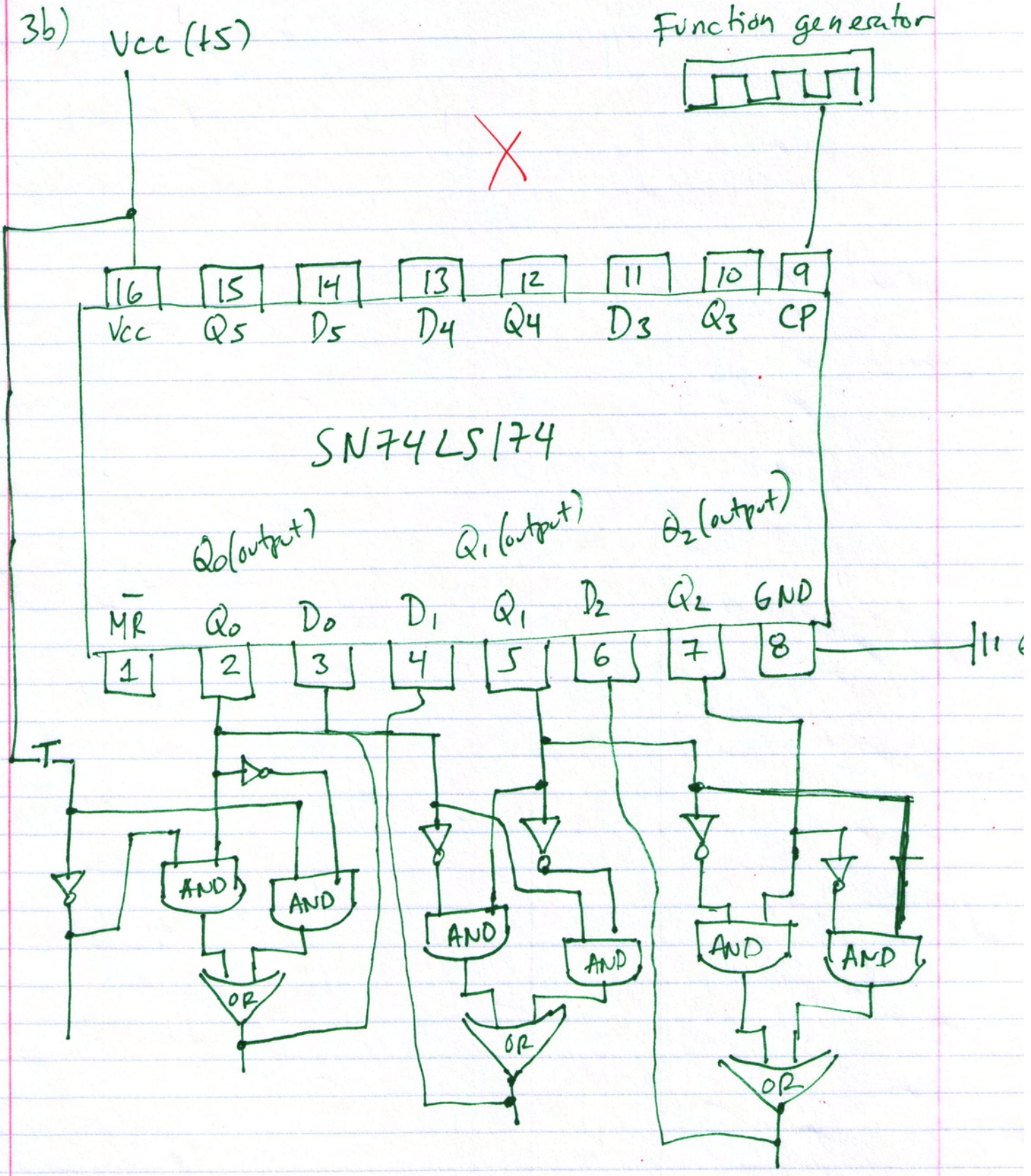
X The problem asks to implement the counter with 74LS174.



In particular the first ff (ϕ) can be done like this:



3b)

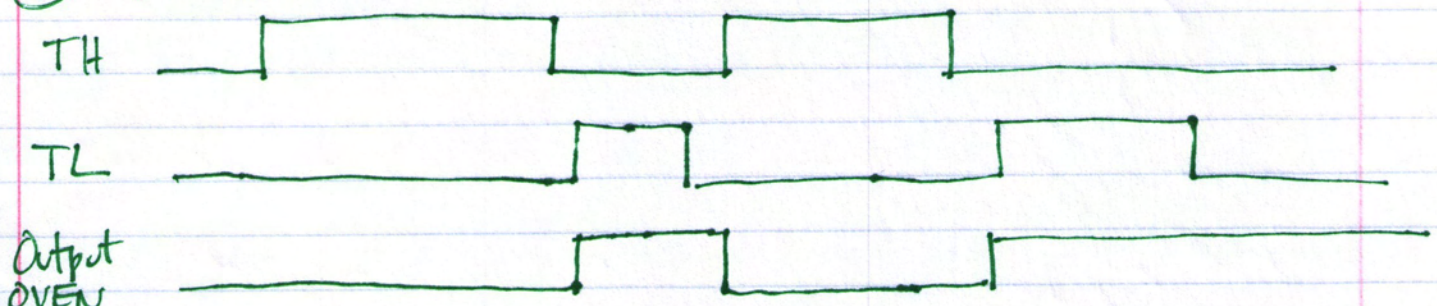

Vcc (+5)
Function generator
16 15 14 13 12 11 10 9
Vcc Q5 D5 D4 Q4 D3 Q3 CP
SN74LS174
Q0 (output)
Q1 (output)
Q2 (output)
MR Q0 D0 D1 Q1 D2 Q2 GND
1 2 3 4 5 6 7 8
T
AND
AND
OR
AND
AND
OR
AND
AND
OR

(4) Frequency = 1 MHz

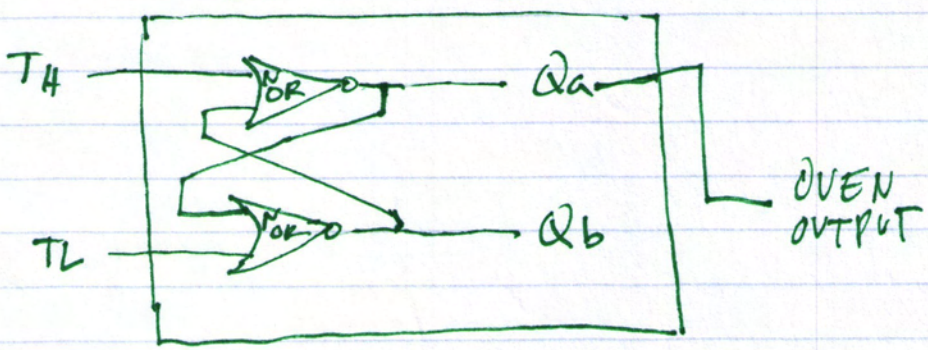
$$\text{Clk period} = \frac{1}{F} = \frac{1}{1\,\text{MHz}} = 1\,\mu s$$ ✓

Worst case for D-Master-Slave to see output change is one clock cycle therefore you will have to wait at most one microsecond.

(5) Waveform (Example)



OVEN ON (1) when TL = 1
OVEN OFF (0) when TH = 1
OTHER WISE NO CHANGE



✓

TL	TH	OVEN OUTPUT
0	0	Previous state (ON/OFF)
0	1	OFF
1	0	ON
1	1	NOT POSSIBLE INPUTS