```
--------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date:   04:07:38 10/08/2007
-- Design Name:   CLA_Adder
-- Module Name:
E:/TRIM/COURSE/545/HOMEWORK/HW4/VHDL/HW4/lookaheadadder_tb.vhd
-- Project Name:  HW4
-- Target Device:
-- Tool versions:
-- Description:
--
-- VHDL Test Bench Created by ISE for module: CLA_Adder
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
-- Notes:
-- This testbench has been automatically generated using types std_logic and
-- std_logic_vector for the ports of the unit under test.  Xilinx recommends
-- that these types always be used for the top-level I/O of a design in order
-- to guarantee that the testbench will bind correctly to the post-implementation
-- simulation model.
--------------------------------------------------------------------------------
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.std_logic_unsigned.all;
USE ieee.numeric_std.ALL;

ENTITY lookaheadadder_tb_vhd IS
END lookaheadadder_tb_vhd;

ARCHITECTURE behavior OF lookaheadadder_tb_vhd IS

        -- Component Declaration for the Unit Under Test (UUT)
        COMPONENT CLA_Adder
        PORT(
                a :   IN std_logic_vector(3 downto 0);
                b :   IN std_logic_vector(3 downto 0);
                cin : IN std_logic;
                s :   OUT std_logic_vector(3 downto 0);
```

```
            cout : OUT std_logic
            );
    END COMPONENT;

    --Inputs
    SIGNAL cin :  std_logic := '0';
    SIGNAL a :  std_logic_vector(3 downto 0) := (others=>'0');
    SIGNAL b :  std_logic_vector(3 downto 0) := (others=>'0');

    --Outputs
    SIGNAL s :  std_logic_vector(3 downto 0);
    SIGNAL cout :  std_logic;

BEGIN

    -- Instantiate the Unit Under Test (UUT)
    uut: CLA_Adder PORT MAP(
            a => a,
            b => b,
            cin => cin,
            s => s,
            cout => cout
    );

    tb : PROCESS
    BEGIN

            -- Wait 100 ns for global reset to finish
            wait for 100 ns;

    --first test the carry in 0
             cin <= '0';
            for I in 0 to 15 loop
            for J in 0 to 15 loop
                    wait for 10 ns;
                    a<=a+"01";
            end loop;
            b<=b+"01";
           end loop;

    --then test the carry in 1
  wait for 100 ns;

              cin <= '1';
            for I in 0 to 15 loop
            for J in 0 to 15 loop
```

```
                wait for 10 ns;
                a<=a+"01";
            end loop;
            b<=b+"01";
           end loop;

        wait; -- will wait forever
    END PROCESS;

END;
```