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-- Company:
-- Engineer:
--
-- Create Date:    03:39:59 10/08/2007
-- Design Name:
-- Module Name:    lookaheadadder - Behavioral
-- Project Name:
-- Target Devices:
-- Tool versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
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----------------------------------------------
LIBRARY ieee;
USE ieee.std_logic_1164.all;
----------------------------------------------
ENTITY CLA_Adder IS

PORT (
                a, b: IN STD_LOGIC_VECTOR (3 DOWNTO 0);
                cin:  IN STD_LOGIC;
                s:    OUT STD_LOGIC_VECTOR (3 DOWNTO 0);
                cout: OUT STD_LOGIC);

END CLA_Adder;
 ----------------------------------------------
 ARCHITECTURE structural OF CLA_Adder IS

        COMPONENT PGU IS
        PORT (
                        a:    IN STD_LOGIC;
                        b:    IN STD_LOGIC;
                  cin : IN  STD_LOGIC;
                        p:    OUT STD_LOGIC;
                        g:    OUT STD_LOGIC;
                        s:    OUT STD_LOGIC
                );
        END COMPONENT;

        COMPONENT CLAU IS
        PORT (
                        cin         :       IN      std_logic;
                        g,p         :       IN      std_logic_vector(3 downto 0);
                        c           :       OUT     std_logic_vector(4 downto 0);
                        cout        :       OUT   std_logic
                );
        END COMPONENT;

 SIGNAL c: STD_LOGIC_VECTOR (4 DOWNTO 0);
 SIGNAL p: STD_LOGIC_VECTOR (3 DOWNTO 0);
```

```
 SIGNAL g: STD_LOGIC_VECTOR (3 DOWNTO 0);

BEGIN
---- PGU: ---------------------------------
G1: FOR i IN 0 TO 3 GENERATE
PGU_UT: PGU port map(
                                        a => a(i),
                                        b => b(i),
                                        cin => c(i),
                                        p => p(i),
                                        g => g(i),
                                        s => s(i)
                                        );
END GENERATE;

CLAU_UT: CLAU port map(
                                                        cin => cin,
                                                        g  => g,
                                                        p  => p,
                                                        c  => c,
                                                        cout => cout
                );


END structural;

---------------------------------------------
LIBRARY ieee;
USE ieee.std_logic_1164.all;
---------------------------------------------
ENTITY PGU IS
PORT (
                        a: IN STD_LOGIC;
                        b: IN STD_LOGIC;
                        cin : IN  STD_LOGIC;
                        p: OUT STD_LOGIC;
                        g: OUT STD_LOGIC;
                        s: OUT STD_LOGIC
        );
END PGU;

ARCHITECTURE structural OF PGU IS

BEGIN
        p <= a XOR b;
        g <= a AND b;
        s <= (a XOR b) XOR cin;
END structural;


---------------------------------------------
LIBRARY ieee;
USE ieee.std_logic_1164.all;
---------------------------------------------
ENTITY CLAU IS
PORT (
```

```
        cin             :   IN      std_logic;
        g,p             :   IN      std_logic_vector(3 downto 0);
        c               :   OUT     std_logic_vector(4 downto 0);
        cout            :  OUT   std_logic
    );
END CLAU;

ARCHITECTURE structural OF CLAU IS

signal c_tmp : std_logic;

BEGIN

    c(0) <= cin;
    c(1) <= (cin AND p(0)) OR g(0);
    c(2) <= (cin AND p(0) AND p(1)) OR (g(0) AND p(1)) OR g(1);
    c(3) <= (cin AND p(0) AND p(1) AND p(2)) OR (g(0) AND p(1) AND p(2)) OR (g(1) AND p(2))
OR g(2);
    c_tmp <= (cin AND p(0) AND p(1) AND p(2) AND p(3)) OR (g(0) AND p(1) AND p(2) AND
p(3)) OR (g(1) AND p(2) AND p(3)) OR (g(2) AND p(3)) OR g(3);
    c(4) <= c_tmp;
    cout <= c_tmp;

END structural;
```