GEORGE MASON UNIVERSITY *ECE 331 Digital System Design* Student:_____

Fall 2007 Nathalia Peixoto

Final Deal

Due **Tuesday**, December 11th at **≤5pm** *(I will leave my office at 5pm sharp – but I will stay there from 3pm to 5pm)*

If you successfully complete this set of problems, you will receive full grade (100) on all homeworks you *turned in* (either on time or up to 1 week late) since the beginning of the semester. There is no second chance: if you show me your work on Dec 11th, and I can't find the solution or how you worked on any particular problem, that's a *NO DEAL*.

Disclaimer: all these problems were either made up by me, or taken from other professors who teach ECE331 or similar courses. If you don't understand the notation, please use your best judgment to come up with a solution (adapt, if necessary).

This final deal is composed of two parts: the first one has 12 problems, numbered 1 through 12. The second is numbered from 1 through 15, starts on page 8 (labeled "Final Deal part II").

1) What are the four methods you can use to describe a logic function?
   a. _____
   b. _____
   c. _____
   d. _____

2) Use the four digits from your date of birth (MMDD, where M=month, D=day) and find:
   a. Decimal representation: _____
   b. Binary representation: _____
   c. 2's complement: _____
   d. 1's complement: _____
   e. Hexadecimal representation: _____
   f. Octal representation: _____
   g. Using the decimal representation, subtract 5000 from (a): _____ (I hope you get a negative number here).
   h. Binary representation: _____
   i. 2's complement: _____
   j. 1's complement: _____
   k. Hexadecimal representation: _____
   l. Octal representation: _____

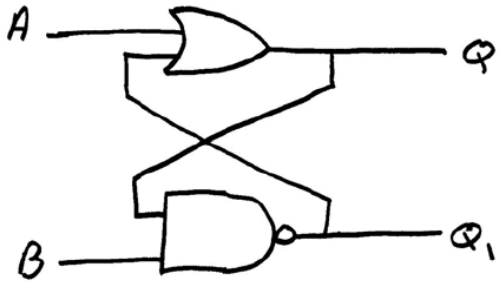
3) Given the function: $F_{w,x,y,z} = \Sigma (0,1,4,5,10,11,14,15)$
   a. Implement it in minimum SOP form, using ONLY the 74LS00.
   b. Is your implementation hazard-free? (explain in written English)
   c. Specify and label each part (you must draw your circuit implementation)
   d. Report the maximum total power dissipated (assume Vcc=5V, Ft=100kHz for each gate; Cl=15pF for each gate; the output of each gate has a 50% duty cycle; Icc values

on the notesheet are for all gates within an entire package, but the dynamic power is calculated for each gate.

e. Determine the SWC and SBC delays.

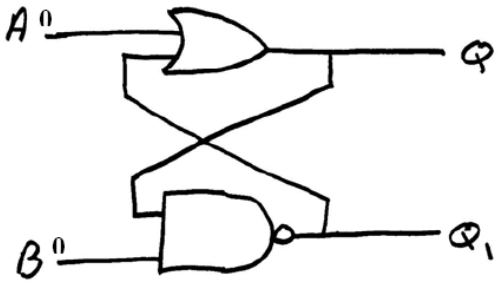
4)

4) *(15 pts)* Determine the output values for Q and Q_1 for each possible input combination. List your results in the table given. Show how you determined your solutions.

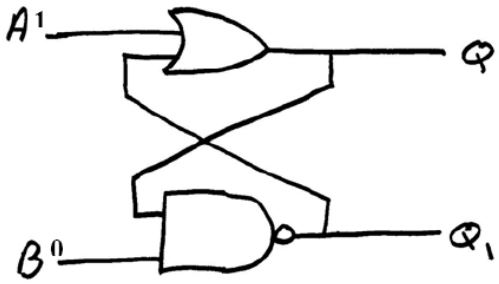


Input Combination A B	Q	Q_1
0 0		
0 1		
1 0		
1 1		

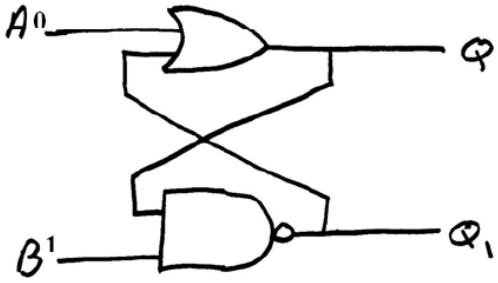
Show work here for A = 0, B = 0:



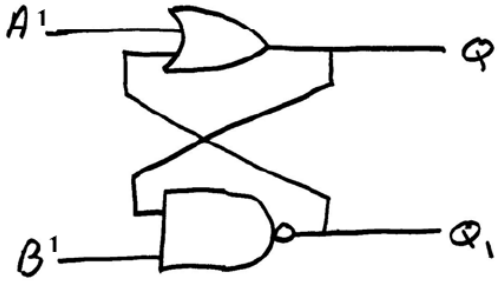
Show work here for A = 1, B = 0:



Show work here for A = 0, B = 1:



Show work here for A = 1, B = 1:

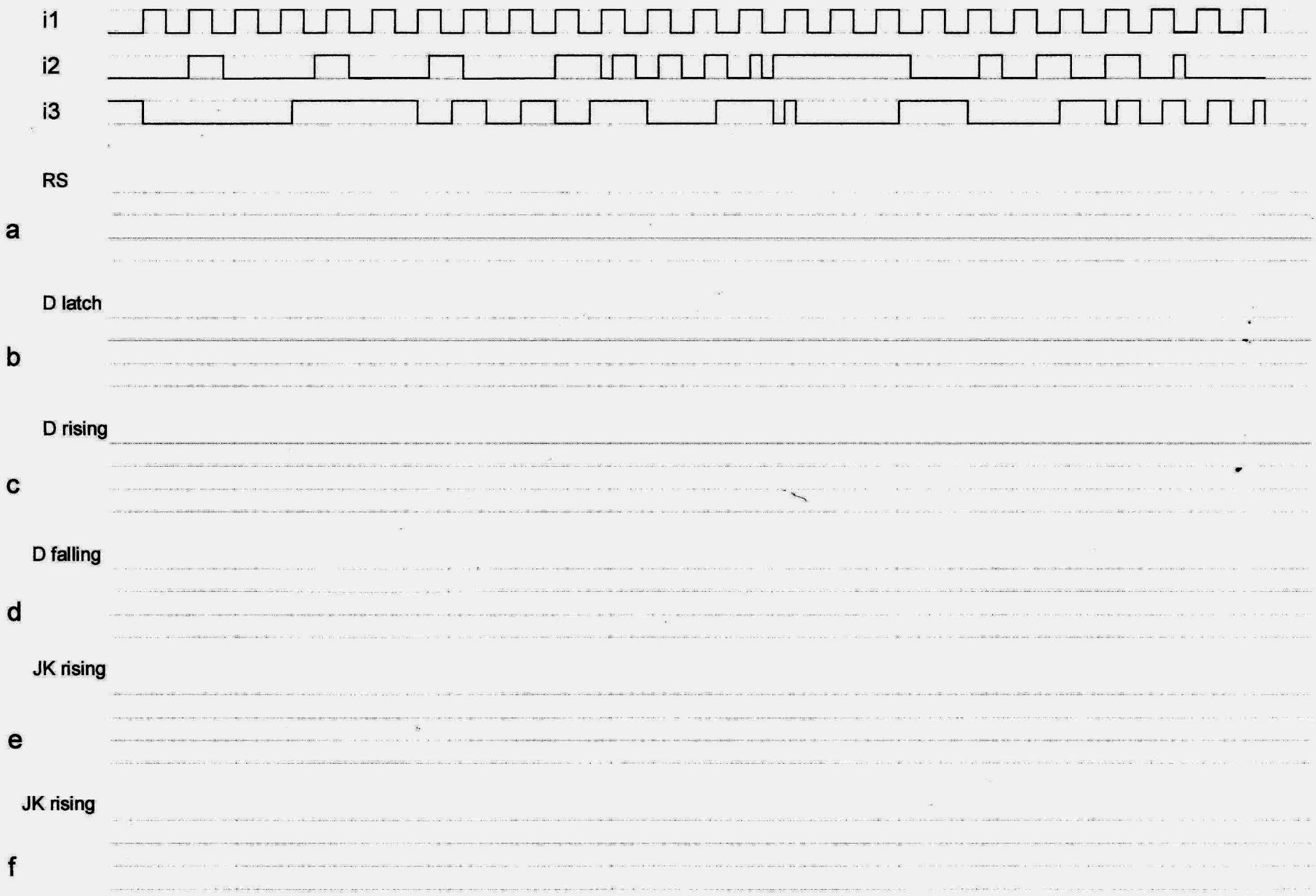


5) Given the graph below (actually in the next page) with i1, i2, and i3 as input signals,
   a. Draw the two outputs of an RS latch with i2 connected to R and i3 connected to S.
   b. Draw the Q and Q' for a D latch if i3 is connected to C and i2 is connected to D.
   c. Draw Q and Q' for a D flip-flop (rising edge) if i1 is connected to Clk and i2 to D.
   d. Draw Q and Q' for a D flip-flop (falling edge) if i1 is connected to Clk and i3 to D.
   e. Draw Q and Q' for a J-K flip-flop (rising edge) if i1 is Clk, i2 is J, i3 is K.
   f. Draw Q and Q' for a J-K flip-flop (rising edge) if i3 is Clk, i1 is J, i2 is K.

   Obs. If you find that i1, i2, and i3 are simultaneously changing state, then assume that i1 has priority over i2, and i2 over i3. That is, if both i1 and i2 are going from 1 to 0 *AT THE SAME TIME*, and you need to decide on the output depending on the timing between these two transitions, assume i1 goes from 1 to 0 *BEFORE* i2 goes from 1 to 0.

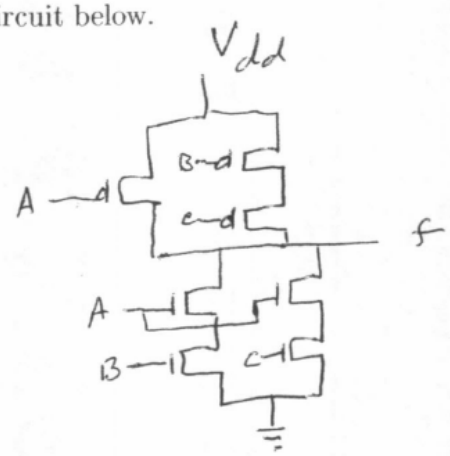
6) You are in the lab, trying to build a state machine with J-K flip-flops. You designed the whole circuitry, based on NAND gates and JK ffs, but when you try to build your machine, you notice you only have D's available (and all the NANDs in the world). Show how you can still build the machine. (In other words: show a diagram of how you can build an edge-triggered J-K from D's and NAND's).

7) Design a two-input, two-output serial subtracter as a Moore state machine. The inputs are series of bits (one bit per clock cycle) beginning with the least-significant bits of the two numbers to be subtracted and the first output is a series of bits representing the difference of the input numbers, presented least significant bit first. The second output is 1 whenever the other output bit represents a digit in the difference, as would be true for all but the reset state.


i1
i2
i3
RS
a
D latch
b
D rising
c
D falling
d
JK rising
e
JK rising
f

8) (CMOS circuit, parts a and b) – number 2 below
9) Sequential x combinational circuit. (number 3 below)

2. [10 Points] Consider the circuit below.



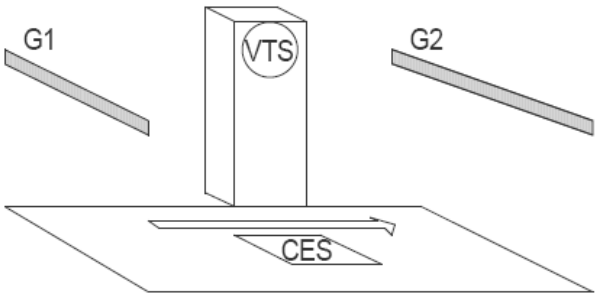
a. (5 points) Give the equation for f.

b. (5 points) This circuit is odd in that the numbers of transistors in the pull-up and pull-down networks are different. Does it matter? Why or why not?

3. [10 points] You are given a schematic diagram of a logic function consisting of interconnected AND, OR, and NOT gates. How would you tell whether the circuit was sequential or combinational?

10 George Mason's new automated parking facilities have recently experienced an increasing loss of revenue because of an inadequate parking gate system. To minimize their losses, Parking Services is looking for an effective alternative gate and control system. Realizing that this is exactly the type of problem which ECE students learn how to solve in ECE331, they have asked you to demonstrate your competence at synchronous FSM design by designing a new parking gate system.

A subcontractor has already installed additional gates, sensors, actuators, and user buttons in addition to the current ticket machine for exiting. The following drawing shows the relative location of the input and output devices.

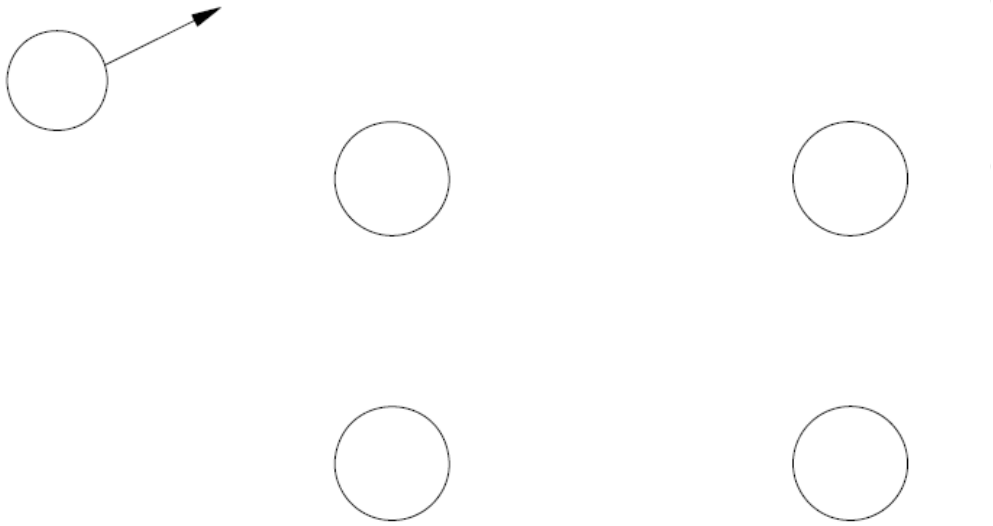


The exit ticket reading machine contains a valid ticket sensor (VTS). The VTS can only be activated once per customer. Whenever a car is over the appropriate exit area next to the ticket machine, a car exit sensor (CES) is activated. The VTS cannot be actuated unless the CES is also actuated. There is no need for you to concern yourself with the internal designs of the ticket machine or the car exit sensor. Both the VTS and CES sensors are asserted as 1.

A gate may be either commanded to open (Gx = 1) or commanded to lock (Gx = 0). There are two gates. Gate One (G1) allows the car to approach the exit machine. Gate Two (G2) is after the ticketing machine and allows the car to exit the parking facility. When there is no car present on the sensor, G2 is closed and G1 remains open. When the CES sensor is activated, G1 closes. Once the CES sensor is activated G2 will only open when the valid ticket sensor (VTS) is activated. After the car exists, the CES sensor deactivates, G2 closes, and G1 opens. Both G1 and G2 should never be open at the same time although one could be closing while the other is opening. For simplicity, ignore the case when a customer comes to the ticket machine and needs to reverse. Assume that there is a sufficient time delay for the car to exit before gate G2 comes down. Assume errored inputs stay in same state.

In order to demonstrate that you alone (this is NOT a group problem) are deserving of full credit for the design of this system:

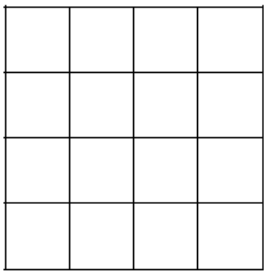
(8) Fill in and properly label the state diagram below to implement the Moore machine showing all of the state transitions for the new parking exit system, including states that are initially assigned "don't know" next states. . Use s_m and s_l as the MSB and LSB present state variables.

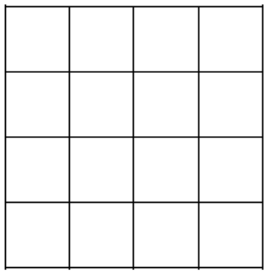


11a (8) Using your state diagram from the previous page, completely fill in the following transition table and determine the output functions and excitation variables. Design using a negative-edge-triggered J-K flip-flop for the MSB and a T flip-flop for the LSB. Complete the state diagram to determine whether or not it is a self-starting machine.

ps/NS (decimal)	MT (hex)	Input		ps		NS		Excitation Variables			Output	
		VTS	CES	s_m	s_l			J_m	K_m	T_l	G1	G2
		0	0	0	0							
		0	0	0	1							
		0	0	1	0							
		0	0	1	1							
		0	1	0	0							
		0	1	0	1							
		0	1	1	0							
		0	1	1	1							
		1	0	0	0							
		1	0	0	1							
		1	0	1	0							
		1	0	1	1							
		1	1	0	0							
		1	1	0	1							
		1	1	1	0							
		1	1	1	1							

11b (2) Use the following Karnaugh maps to minimize the function specified. Write the minterms in the space provided.





$J_m = \Sigma_1(\quad) + \Sigma_d(\quad)$ $T = \Sigma_1(\quad) + \Sigma_d(\quad)$

12) Present a hazard-free implementation of the following functions:

a) In SOP format: A x,y,z,w = Σ(3-7,12,15)

b) In POS format: Xa,b,c,d = π (0,2,6,9,13,14)+d(5,7,8).

Final Deal part II

1) *(10 pts)* Determine the Boolean equation for the minimum **POS** static-hazard-free implementation of the function $F_{A,B,C,D} = \Sigma(1, 6, 9–11, 14)$. Show how you determined this implementation.

   You need **not** draw the resultant logic circuit.

2) *(10 pts)* For the pair of decimal values A and B in the table below, (*i*) express each number in the 1's complement system in columns 3 and 4, respectively, **using 8 bits** (*ii*) express each number in the 2's complement system in columns 5 and 6, respectively, **using 8 bits** and (*iii*) express their sum and difference in the 2's complement system in columns 7 and 8, respectively, **using 8 bits.**

   In all cases, write a result as "OVERFLOW" if it cannot be contained in the 8-bit representation.

Decimal Value:		**1's Comp. Number System (8 Bits)**		**2's Comp. Number System (8 Bits)**			
A	**B**	**A**	**B**	**A**	**B**	**A + B**	**A – B**
-97	30						

3) *(15 pts)* Use basic logic gates (AND, OR, NOT — any number of inputs) to **design** a **minimum SOP** combinational logic circuit to add a **two-bit** unsigned binary number (e.g. $00_2 \rightarrow 0_{10}$, $01_2 \rightarrow 1_{10}$, $10_2 \rightarrow 2_{10}$ and $11_2 \rightarrow 3_{10}$) to a **one-bit** unsigned binary number, with sufficient output bit length to contain any result.

   Your **design** should be a three-input (two bits for the two-bit unsigned integer and one bit for the one-bit unsigned integer), three-output (for the three-bit unsigned integer sum) combinational logic circuit. (Note that overflow is not possible.)

   Show your truth table, method of logic function minimization, and final logic equations for your outputs. To save time, you need **not** draw the resultant logic circuit.

use 74F00 only

4) *(15 pts)* Using only the six basic "Fast TTL" ICs listed on the exam notesheet (use the specs from this sheet as well), **implement** the function below while minimizing (*i*) maximum total power dissipated (assume V_{CC} = 5 V; and the output of each gate spends half of its time high — remember that the I_{CC} values on the notesheet are for an entire package) and (*ii*) the worst-case propagation delay.

In your design, (*i*) specify and label each part **(you must draw your circuit implementation)**, (*ii*) report the maximum total power dissipated and (*iii*) report the worst-case propagation delay.

Function: $\mathbf{F_{W,X,Y,Z} = \Sigma(3\text{–}7, 11, 15)}$.

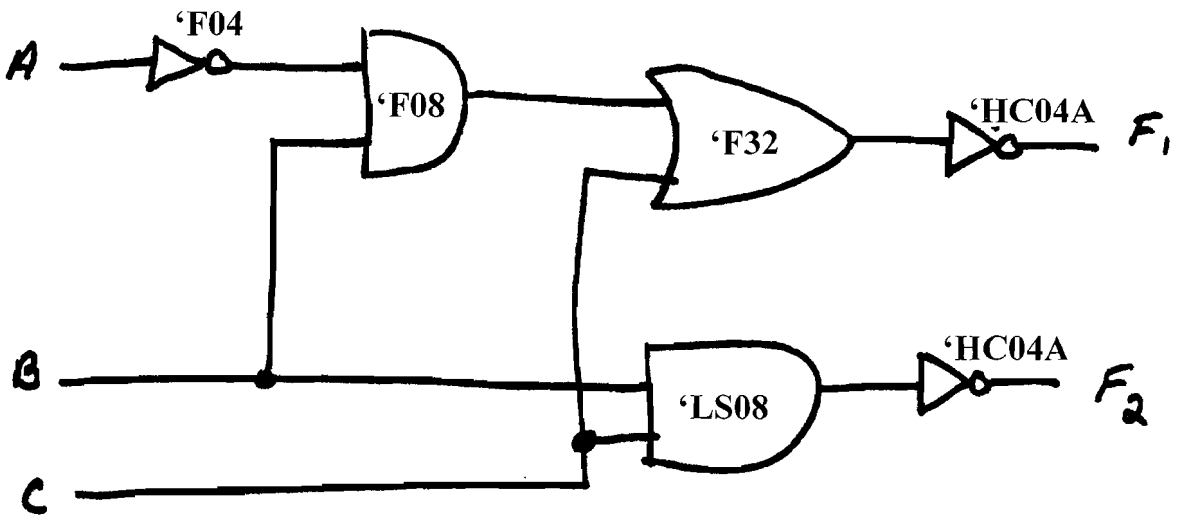
5) *(10 pts)* Determine the fanout limit when a Motorola 74HC00A NAND Gate (CMOS) drives a Motorola 74F32 OR Gate (FAST TTL).

6) *(10 pts)* For the **Motorola 74HC08A**, determine the **maximum** quiescent power dissipation, dynamic power dissipation and total power dissipation when one gate from the IC drives a capacitive load of C_L = 20 pF at a switching frequency of 10 kHz, when powered by a 5 V source. Assume the gate output spends 50% of its time in the high output state and 50% of its time in the low output state.

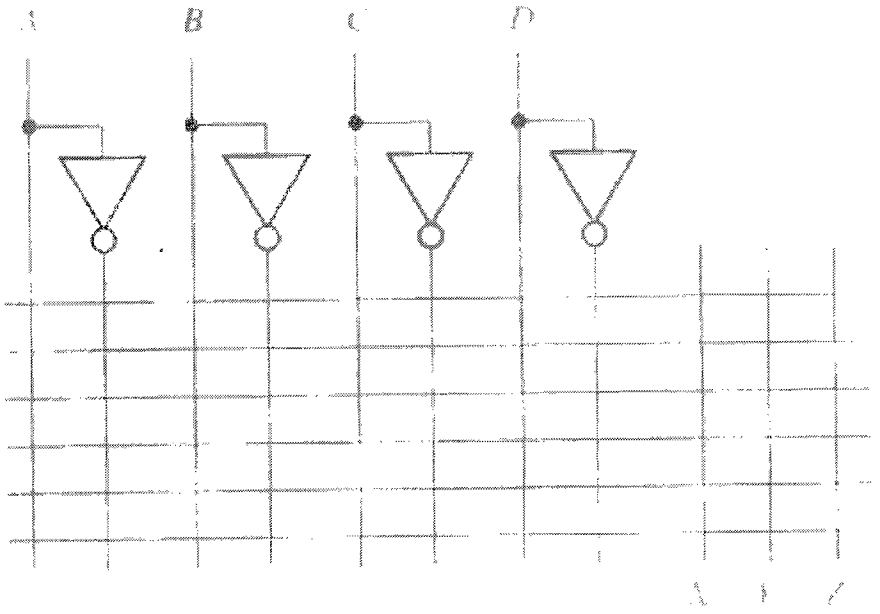
7) *(10 pts)* Use the Sum of Worst Case (SWC) analysis technique to determine the maximum propagation delay for the circuit shown below. ***Show how you determined this value.***

- For Fast TTL parts ("'Fyy"), use Motorola MC74Fyy parts.
- For LS TTL parts ("'LSxx"), use Motorola SN74LSxx parts.
- For CMOS parts ("'HCzz"), use Motorola 74HCzz parts.

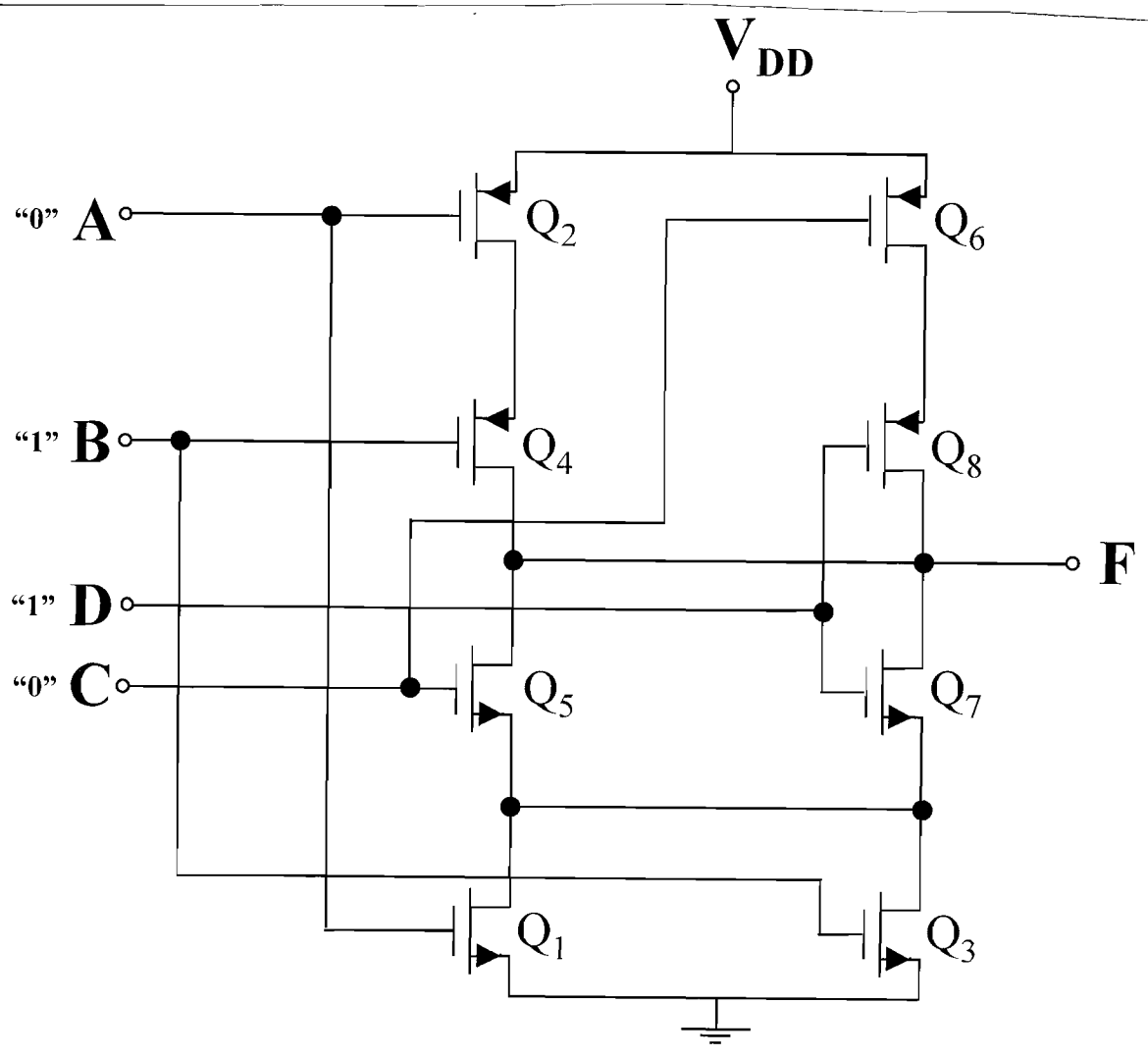
All necessary specifications should be available on your test notesheet.



8) *(10 pts)* Use the "short hand" notation for showing the programming of the PLA below to implement: $X_{A, B, C, D} = \Sigma\ (3, 6, 11, 15)$.



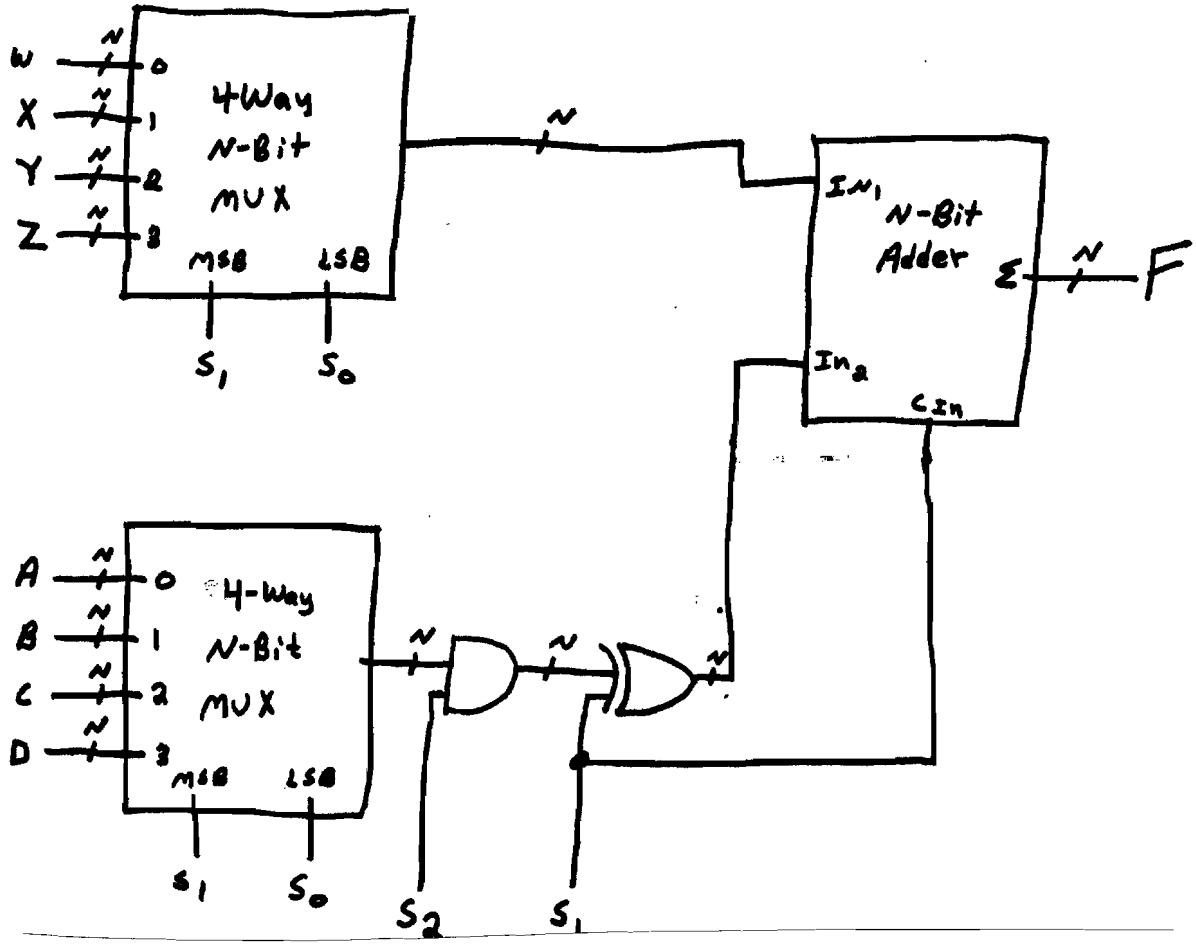
9) *(15 pts)* Determine the ON/OFF state of each transistor (Q1 through Q8) and the logic value of the output in the CMOS circuit shown below when: A = 0, B = 1, C = 0, and D = 1 (logic levels).



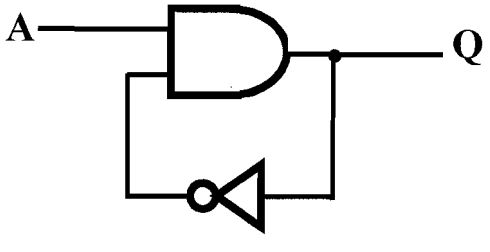
10) *(15 pts)* The ALU below has N-bit 2's complement data inputs W, X, Y, Z, A, B, C and D; control input bits S_0, S_1 and S_2; and an N-bit data output F. The XOR and AND gates each represent N gates (one per bit), respectively.

Determine the arithmetic function performed by this ALU for each of the eight possible control inputs shown in the Instruction Code table.

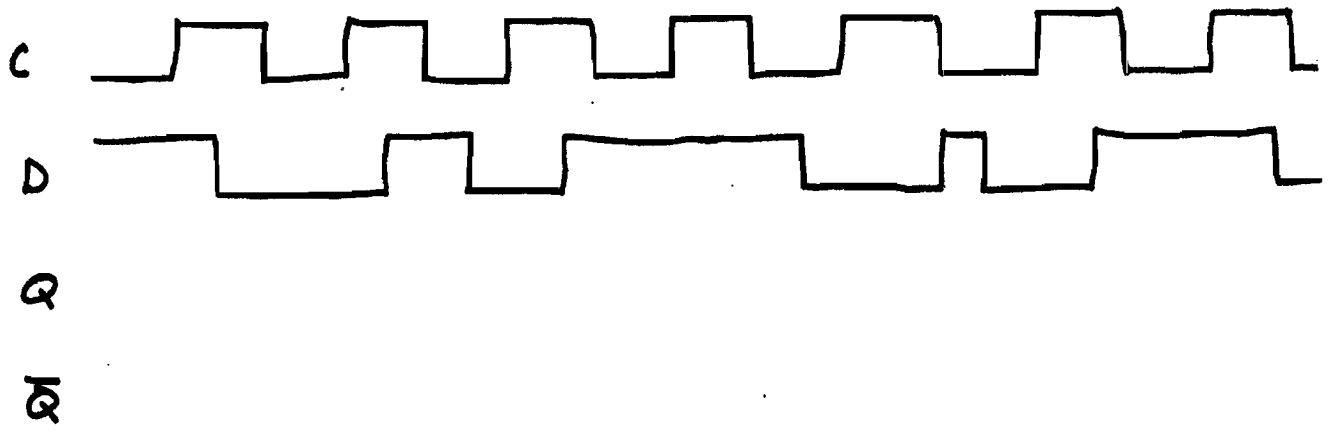
Instruction Code $S_2\ S_1\ S_0$	Function F = ?
0 0 0	
0 0 1	
0 1 0	
0 1 1	
1 0 0	
1 0 1	
1 1 0	
1 1 1	



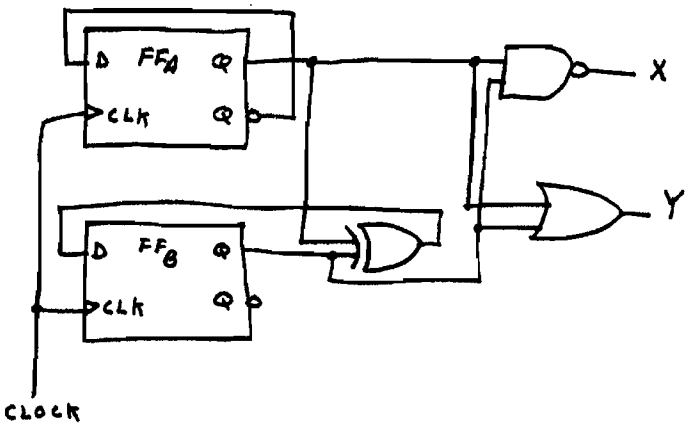
11) *(10 pts)* The circuit below (with input "A" and output "Q") utilizes feedback. Describe, in words (written English!), the operation of the circuit separately for the cases when A = 0 (logic low) and A = 1 (logic high).



12) *(10 pts)* The figure below shows a partial timing diagram. Draw the corresponding timing diagrams for the two resulting output waveforms Q and Q', if C and D are the inputs to an **edge-triggered D flip-flop**.

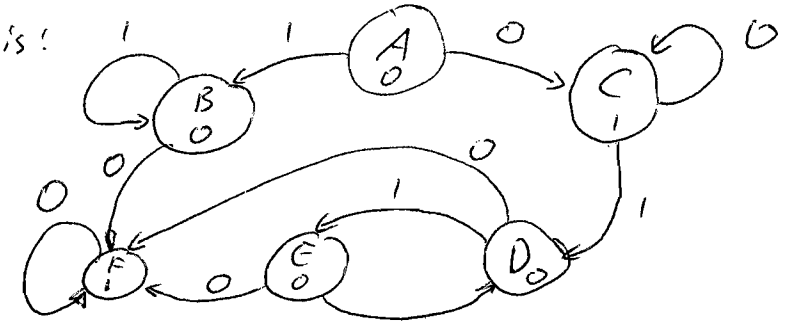


13) *(15 pts)* Analyze the sequencer shown below using the four-step process to *i*) Identify the next state and output logic, *ii*) Write the output and next state equations, *iii*) Construct the Transition Table and *iv*) Construct the State Transition Diagram.



14) Design a State Machine of type Mealy that detects the sequence "1101". Use JK Flip-Flops.

15) Minimize this!



Which sequence does it detect?